

General Description

SFGMOS[®]

$R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. The high V_{th} series is specially optimized for high systems with gate driving voltage greater than 10V.

Features

- Low $R_{DS(ON)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity
- Fast switching and soft recovery



Applications

- Switched mode power supply
- Motor driver
- Battery protection
- DC-DC convertor
- Solar inverter
- UPS and energy inverter

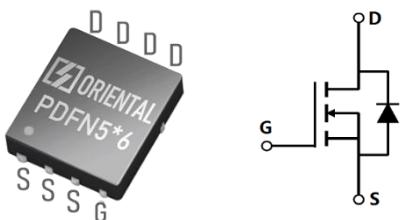
Key Performance Parameters

Parameter	Value	Unit
$V_{DS, min} @ T_{j(max)}$	100	V
$I_D, pulse$	300	A
$R_{DS(ON), max} @ V_{GS}=10V$	8	
Q_g	55.6	nC

Marking Information

Product Name	Package	Marking
SFG100N10GF	PDFN5*6	SFG100N10G

Package & Pin information



Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	100	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾ , $T_C=25^\circ\text{C}$	I_D	100	A
Pulsed drain current ²⁾ , $T_C=25^\circ\text{C}$	$I_{D,\text{pulse}}$	300	A
Continuous diode forward current ¹⁾ , $T_C=25^\circ\text{C}$	I_S	100	A
Diode pulsed current ²⁾ , $T_C=25^\circ\text{C}$	$I_{S,\text{pulse}}$	300	A
Power dissipation ³⁾ , $T_C=25^\circ\text{C}$	P_D	148	W
Single pulsed avalanche energy ⁵⁾	E_{AS}	130	mJ
Operation and storage temperature	$T_{\text{stg}} \quad T_j$	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	R	0.84	°C/W
Thermal resistance, junction-ambient ⁴⁾	R	62	°C/W

Electrical Characteristics at $T_j=25^\circ\text{C}$ unless otherwise specified en-US

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	100			V	$V_{GS}=0 \text{ V}$, $I_D=250 \text{ A}$
Gate threshold voltage	$V_{GS(\text{th})}$	2.0		4.0	V	$V_{DS}=V_{GS}$, $I_D=250 \text{ A}$
Drain-source on-state resistance	$R_{DS(\text{ON})}$		6.5	8.0		$V_{GS}=10 \text{ V}$, $I_D=12 \text{ A}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20 \text{ V}$

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C _{iss}		3530		pF	V _{GS} =0 V, V _{DS} =50 V, 1 MHz
Output capacitance	C _{oss}		560		pF	
Reverse transfer capacitance	C _{rss}		9		pF	
Turn-on delay time	t _{d(on)}		22.5		ns	V _{GS} =10 V, V _{DS} =50 V, R _G I _D =10 A
Rise time	t _r		8.6		ns	
Turn-off delay time	t _{d(off)}		66.6		ns	
Fall time	t _f		42.1		ns	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q _g		55.6		nC	V _{GS} =10 V, V _{DS} =50 V, I _D =10 A
Gate-source charge	Q _{gs}		14.9		nC	
Gate-drain charge	Q _{gd}		11.2		nC	
Gate plateau voltage	V _{plateau}		4.7		V	

Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward voltage	V _{SD}			1.3	V	I _S =30 A, V _{GS} =0 V
Reverse recovery time	t _{rr}		67		ns	V _R =50 V, I _S =10 A,
Reverse recovery charge	Q _{rr}		160		nC	
Peak reverse recovery current	I _{rrm}		3.9		A	

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) Pd is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of R_d is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_a=25 °C.
- 5) V_{DD}=50 V, V_{GS}=10 V, L=0.3 mH, starting T_j=25 °C.

Electrical Characteristics Diagrams

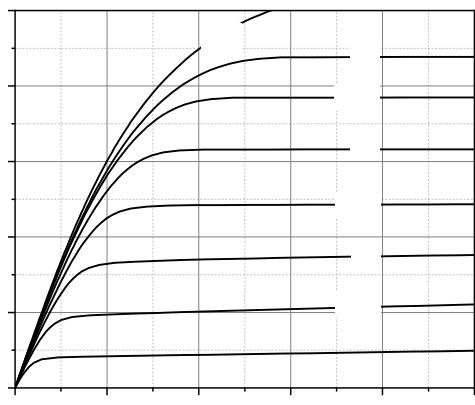


Figure 1. Typ. output characteristics

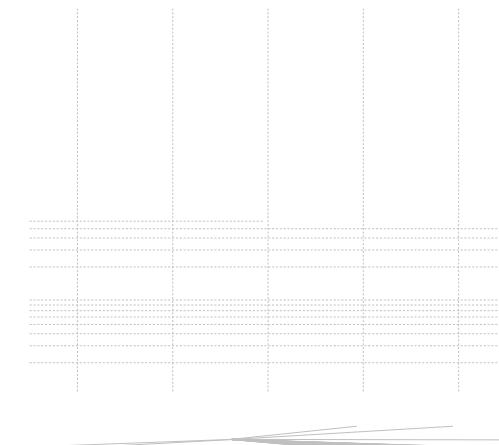


Figure 2. Typ. transfer characteristics

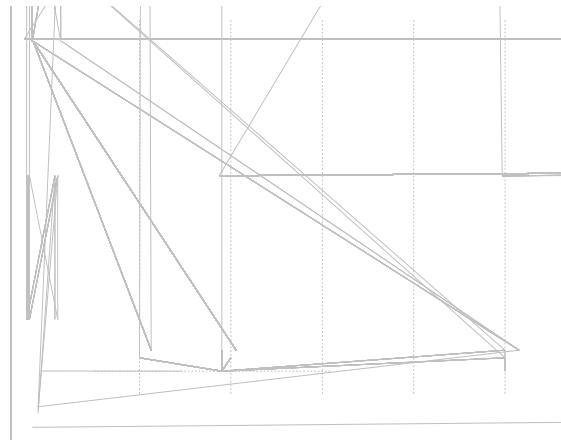


Figure 3. Typ. capacitances

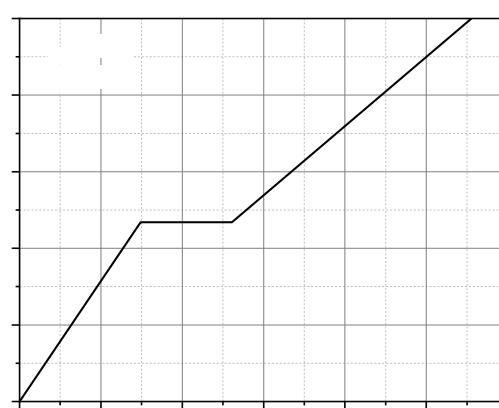


Figure 4. Typ. gate charge

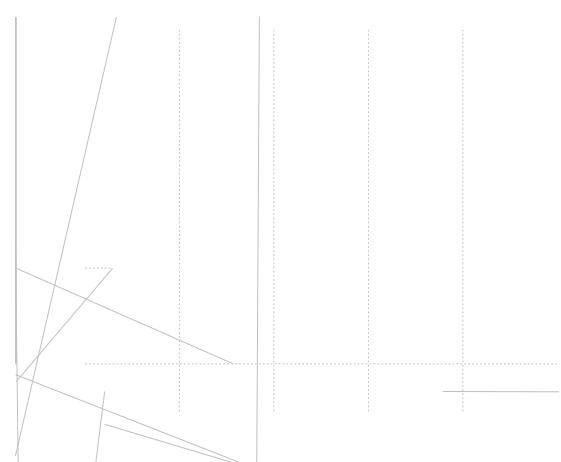


Figure 5. Drain-source breakdown voltage

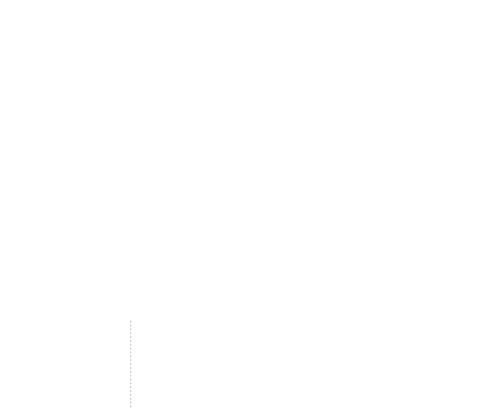


Figure 6. Drain-source on-state resistance

Test circuits and waveforms

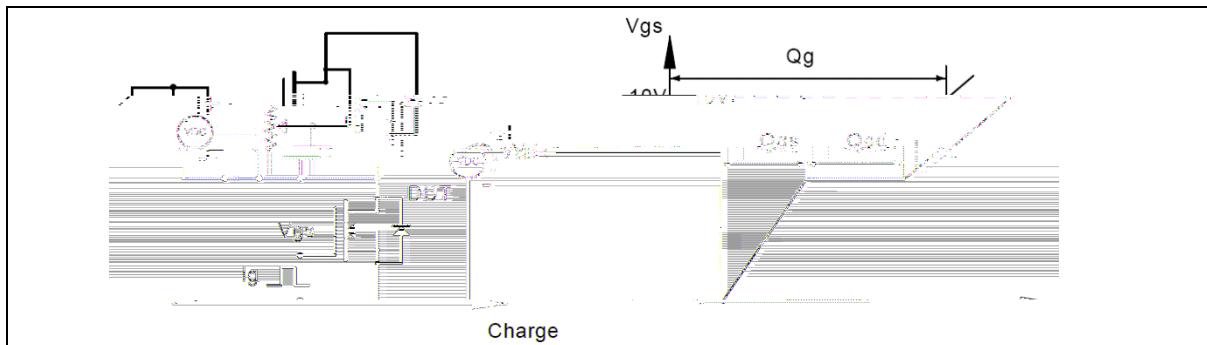


Figure 1. Gate charge test circuit & waveform

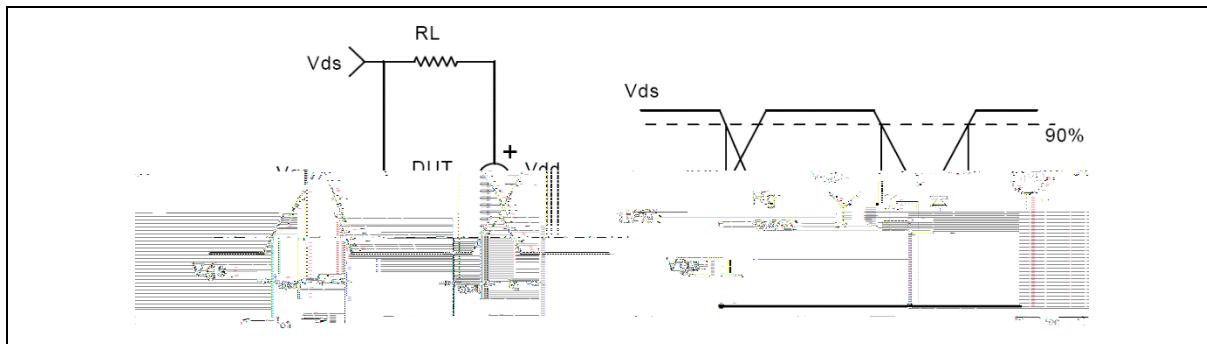


Figure 2. Switching time test circuit & waveform

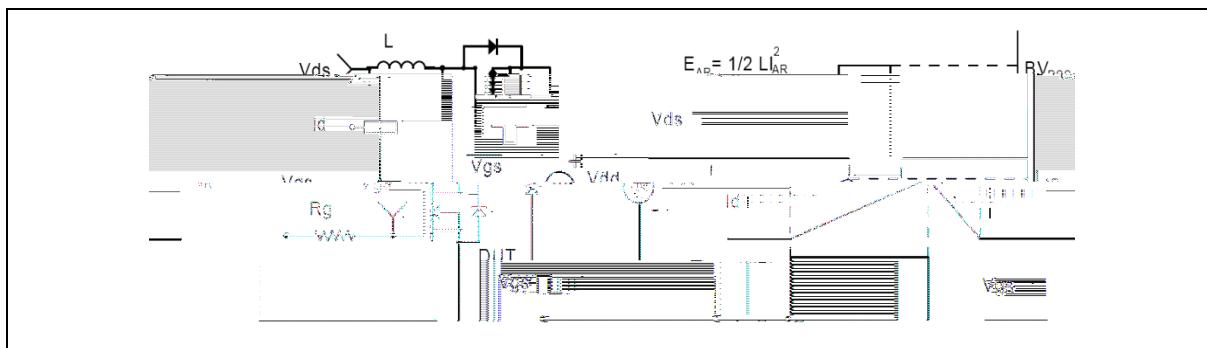


Figure 3. Unclamped inductive switching (UIS) test circuit & waveform

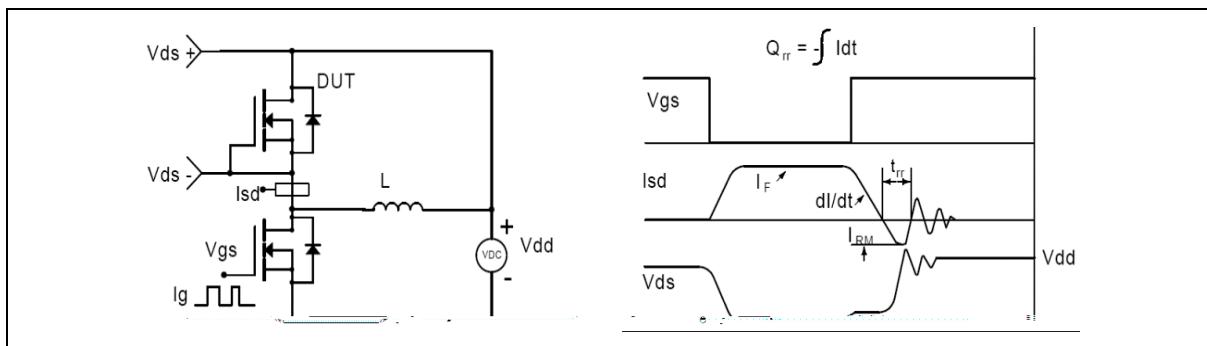
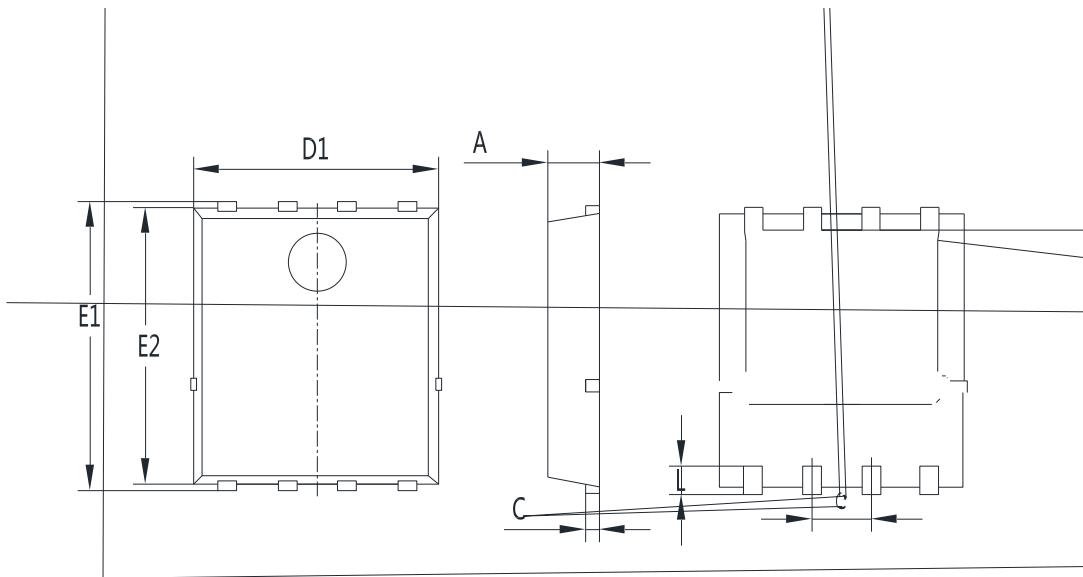


Figure 4. Diode reverse recovery test circuit & waveform

Package Information



Symbol	mm		
	Min	Nom	Max
A	1.00	1.10	1.20
b	0.30	0.40	0.50
c	0.154	0.254	0.354
D1	5.00	5.20	5.40
D2	3.80	4.10	4.25
e	1.17	1.27	1.37
E1	5.95	6.15	6.35
E2	5.66	5.86	6.06
E4	3.52	3.72	3.92
H	0.40	0.50	0.60
L	0.30	0.60	0.70
L1	0.12 REF		
K	1.15	1.30	1.45

Version 1: PDFN5*6-C package outline dimension

Package Information



Symbol	mm		
	Min	Nom	Max
A	0.8	0.9	1.0
A1	0	0.03	0.05
b	0.35	0.42	0.49
c	0.254 REF		
D	4.9	5.0	5.1
F	1.40 REF		
E	5.7	5.8	5.9
e	1.27 BSC		
H	5.95	6.08	6.20
L1	0.10	0.14	0.18
G	0.60 REF		
K	4.00 REF		

Version 2: PDFN5*6-K package outline dimension

Ordering Information

Package Type	Units/Reel	Reels / Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
PDFN5*6-C	5000	2	10000	5	50000
PDFN5*6-K	5000	2	10000	5	50000

Product Information

Product	Package	Pb Free	RoHS	Halogen Free
SFG100N10GF	PDFN5*6	yes	yes	yes

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