General Description

SFGMOS®

$R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. The high V_{th} series is specially optimized for high systems with gate driving voltage greater than 10V.

Features

- Low $R_{DS(ON)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity
- Fast switching and soft recovery

RoHS compliant

Applications

- Switched mode power supply
- Motor driver
- Battery protection
- DC-DC convertor
- Solar inverter
- UPS and energy inverter

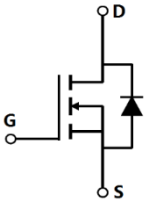
Key Performance Parameters

Parameter	Value	Unit
$V_{DS,\ min}$ @ $T_{j(max)}$	80	V
$I_{D,\ pulse}$	300	A
$R_{DS(ON),\ max}$ @ V_{GS}=10V	5.9	
Q_g	53.2	nC

Marking Information

Product Name	Package	Marking
SFG100N08GF	PDFN5*6	SFG100N08G

Package & Pin information



Absolute Maximum Ratings at T_j=25°C unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	80	V
Gate source voltage	V_{GS}	±20	V
Continuous drain current[1)], T_C=25 °C	I_D	100	A
Pulsed drain current[2)], T_C=25 °C	$I_{D, pulse}$	300	A
Continuous diode forward current[1)], T_C=25 °C	I_S	100	A
Diode pulsed current[2)], T_C=25 °C	$I_{S, pulse}$	300	A
Power dissipation[3)], T_C=25 °C	P_D	148	W
Single pulsed avalanche energy[5)]	E_{AS}	135	mJ
Operation and storage temperature	T_{stg} T_j	-	

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		4242		pF	V_{GS}=0 V, V_{DS}=25 V, 100 kHz
Output capacitance	C_{oss}		1779		pF	
Reverse transfer capacitance	C_{rss}		84.1		pF	
Turn-on delay time	$t_{d(on)}$		28		ns	V_{GS}=10 V, V_{DS}=40 V, R_G I_D=50 A
Rise time	t_r		6.5		ns	
Turn-off delay time	$t_{d(off)}$		48.5		ns	
Fall time	t_f					

Electrical Characteristics Diagrams

Figure 7. Threshold voltage

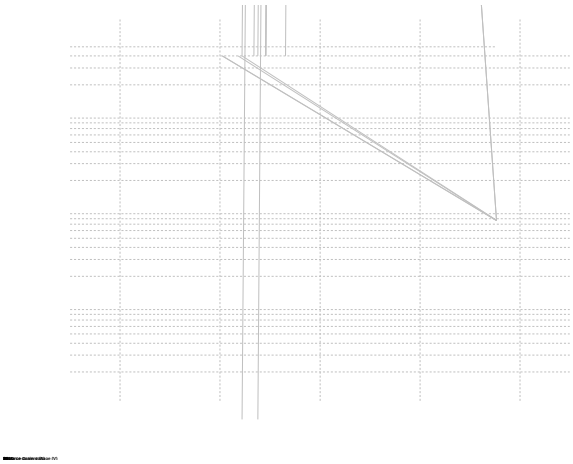


Figure 8. Forward characteristic of body diode

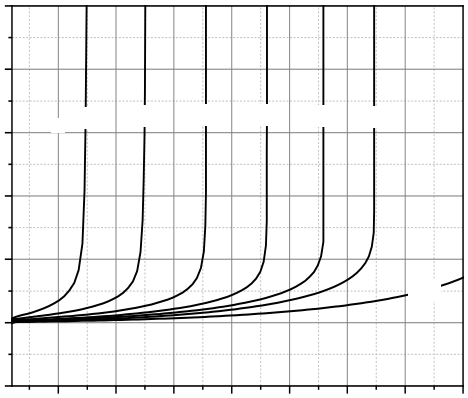


Figure 9. Drain-source on-state resistance

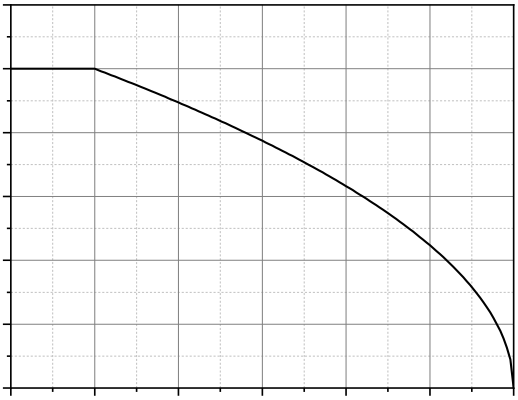


Figure 10. Drain current

Figure 11. Safe operation area T_C=25 °C

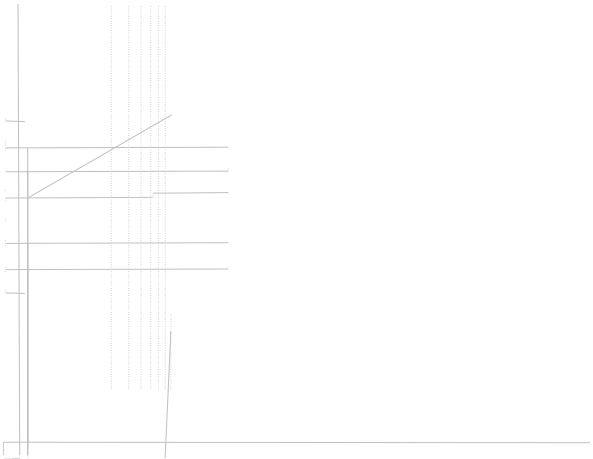


Figure 12. Max transient thermal impedance

Test circuits and waveforms

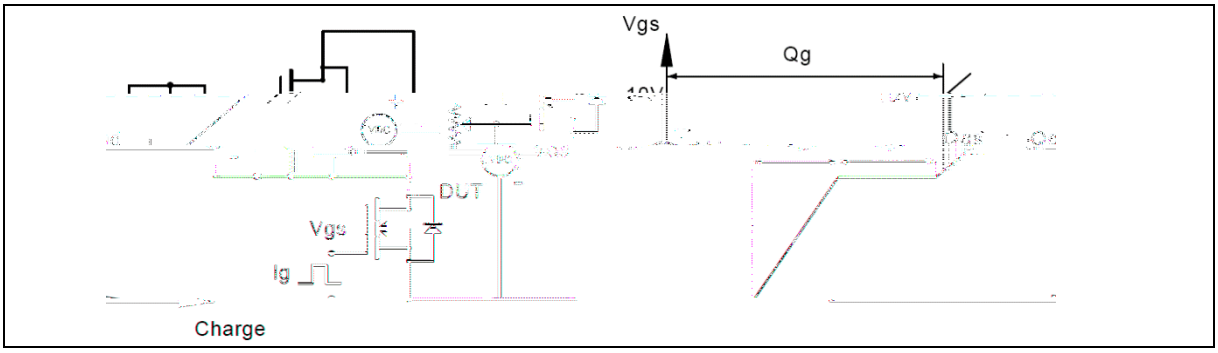


Figure 1. Gate charge test circuit & waveform

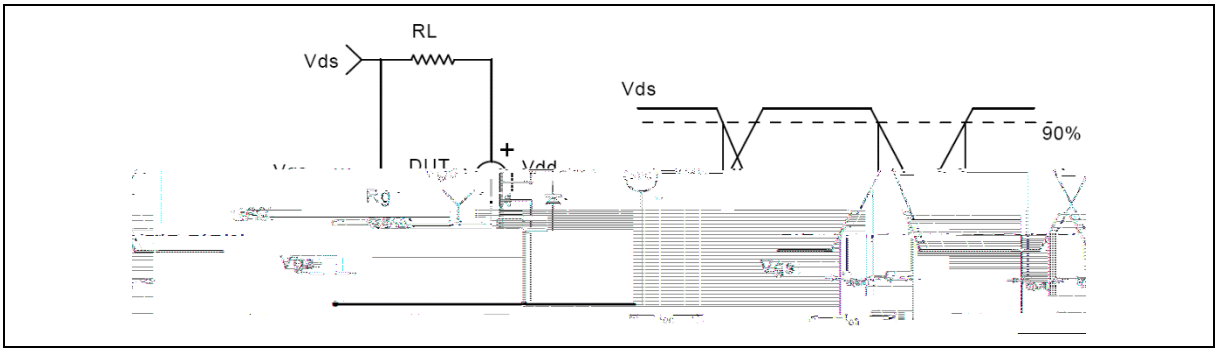


Figure 2. Switching time test circuit & waveforms

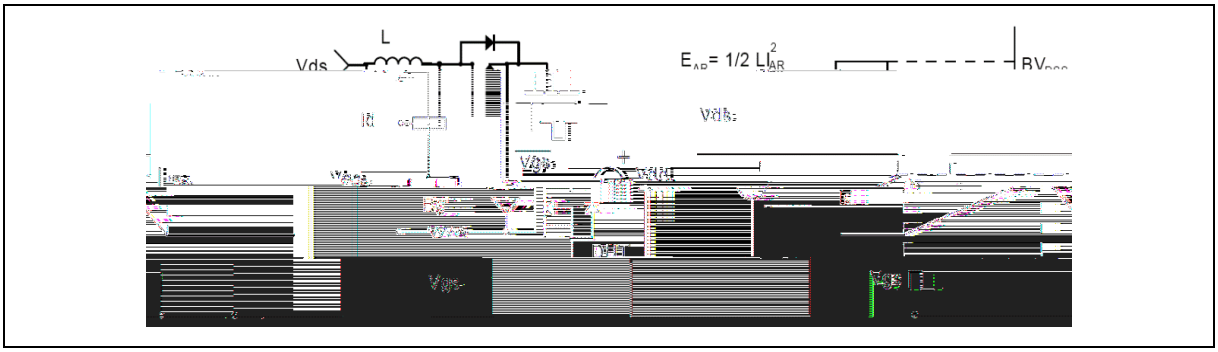


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

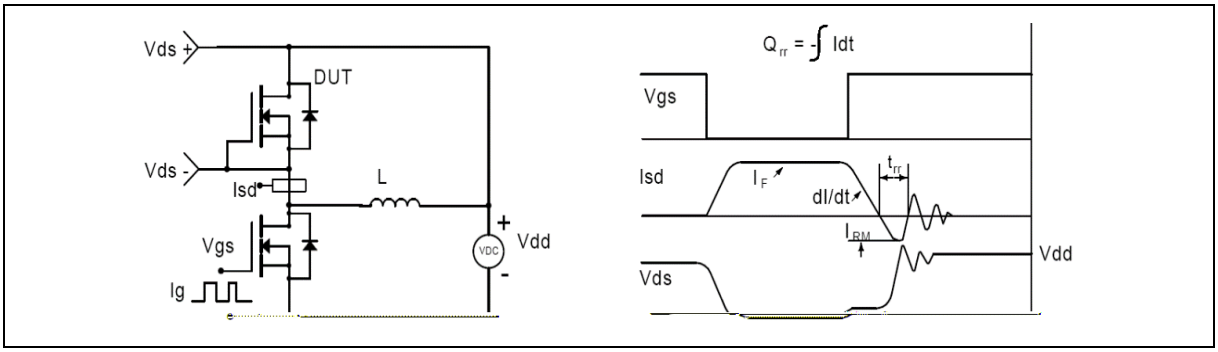


Figure 4. Diode reverse recovery test circuit & waveforms

Package Information

Symbol	mm		
	Min	Nom	Max
A	1.00	1.10	1.20
b	0.30	0.40	0.50
c	0.154	0.254	0.354
D1	5.00	5.20	5.40
D2	3.80	4.10	4.25
e	1.17	1.27	1.37
E1	5.95	6.15	6.35
E2	5.66	5.86	6.06
E4	3.52	3.72	3.92
H	0.40	0.50	0.60
L	0.30	0.60	0.70
L1	0.12 REF		
K	1.15	1.30	1.45

Version 1: PDFN5*6-C package outline dimension