

NABHJN HJNA@ th n ji Jndio gN hdji p qm pi d p qd n d i q cdq gr
M NJI gr b o c r b a n n r d c d b i s g r i o q g i c c m o n (d n) O c c d c Q a n n d n
d n k d g j k a d d a j m d c n t n o h n r d c b o n d b q j d b b m o m a i , Q)

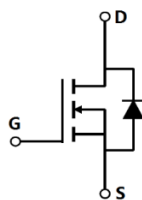
- G r M NJI ! A J H
- @ s m h g g r n r d c d b g n n
- @ g r i o m d d i p i d i r h d d
- A n n r d c d b i n j a m j q r h



- N r d c h j k j r m p k k g
- H j q m n d m
- = d r h k n j o d j i
- - j i q n j m
- Solar inverter
- P K N i i r b t d i q n o m

Parameter	Value	Unit
$V_{DS, min} @ T_{j(max)}$	100	V
$I_D, pulse$	390	A
$R_{DS(ON), max} @ V_{GS}=10V$	5	Ω
Q_g	91.7	nC

Product Name	Package	Marking
SFG10R05FF	TO220F	SFG10R05F



Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		6388.6		pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, 8, Hz
Output capacitance	C_{oss}		923.3		pF	
Reverse transfer capacitance	C_{rss}		1.4		pF	
Turn-on delay time	$t_{d(on)}$		30.9		ns	$V_{GS}=10\text{ V}$, $V_{DS}=50\text{ V}$, $R_{\theta 8-}$ $I_D=25\text{ A}$
Rise time	t_r		10.0		ns	
Turn-off delay time	$t_{d(off)}$		66.8		ns	
Fall time	t_f		12.5		ns	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q_g		91.7		nC	$V_{GS}=10\text{ V}$, $V_{DS}=50\text{ V}$, $I_D=25\text{ A}$
Gate-source charge	Q_{gs}		23.7		nC	
Gate-drain charge	Q_{gd}		22.3		nC	
Gate plateau voltage	$V_{plateau}$		4.8		V	

1)

Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward voltage	V_{SD}			1.3	V	$I_S=20\text{ A}$, $V_{GS}=0\text{ V}$
Reverse recovery time	t_{rr}		88.0		ns	$I_S=25\text{ A}$, $d\ \varnothing$, n
Reverse recovery charge	Q_{rr}		273		nC	
Peak reverse recovery current	I_{rrm}		5.2		A	

Note

1) 1) Calculated continuous current based on maximum allowable junction temperature.

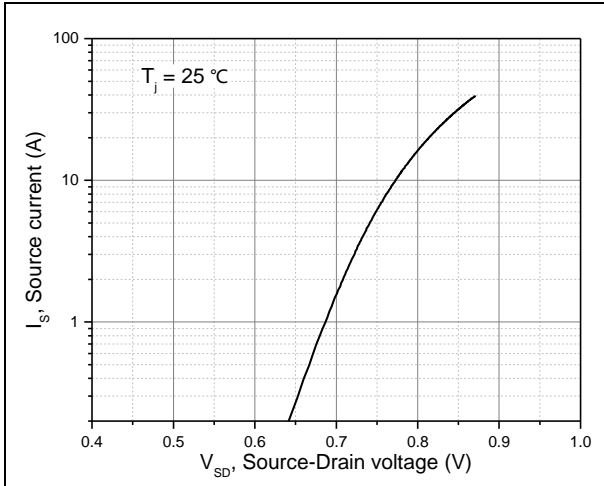


Figure 7. Forward characteristic of body diode

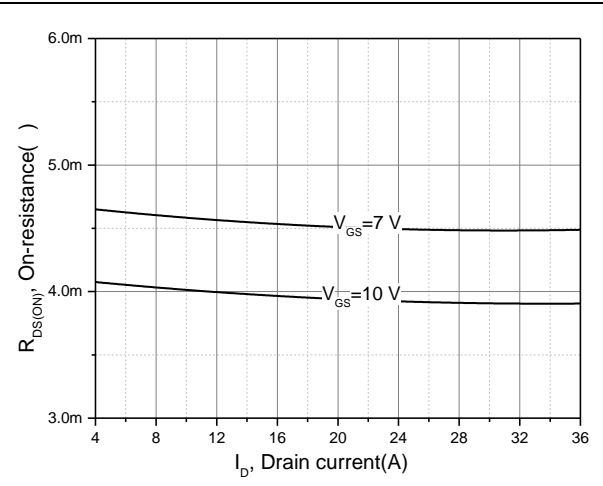


Figure 8. Drain-source on-state resistance

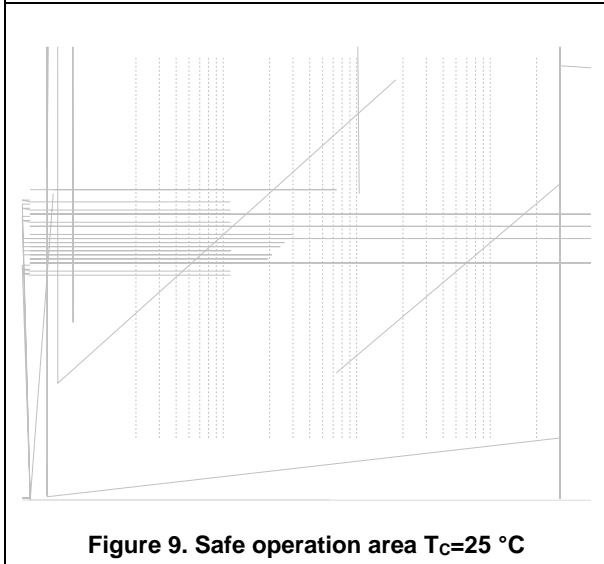


Figure 9. Safe operation area $T_C=25\text{ }^\circ\text{C}$

Test circuits and waveforms

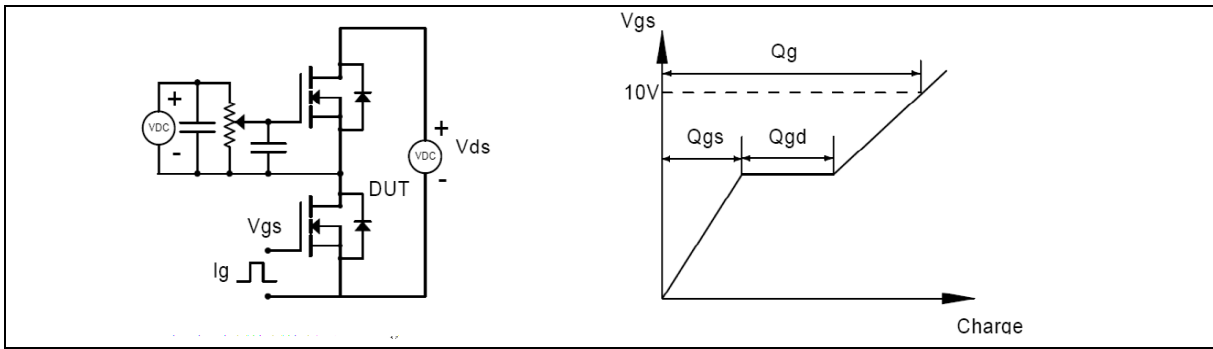


Figure 1. Gate charge test circuit & waveform



Figure 2. Switching time test circuit & waveforms

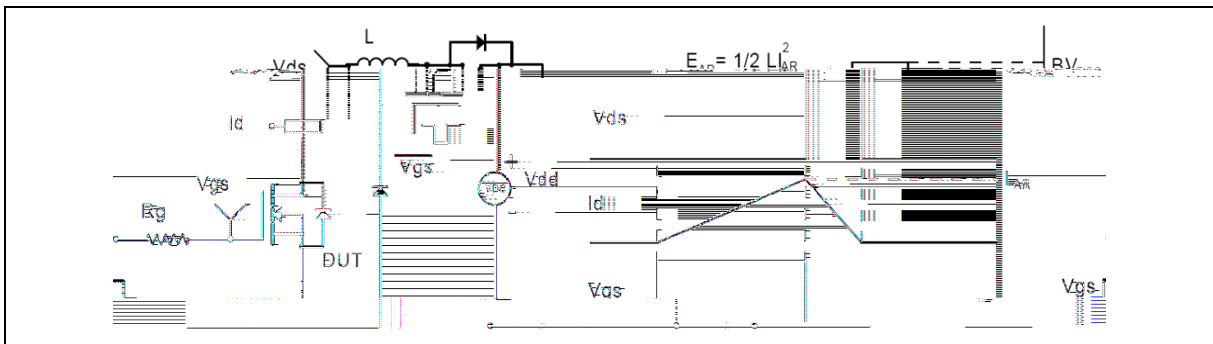


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

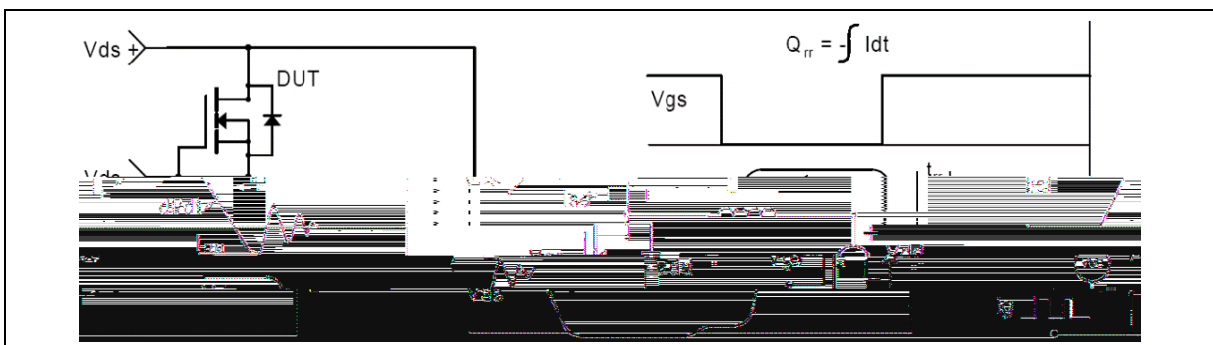
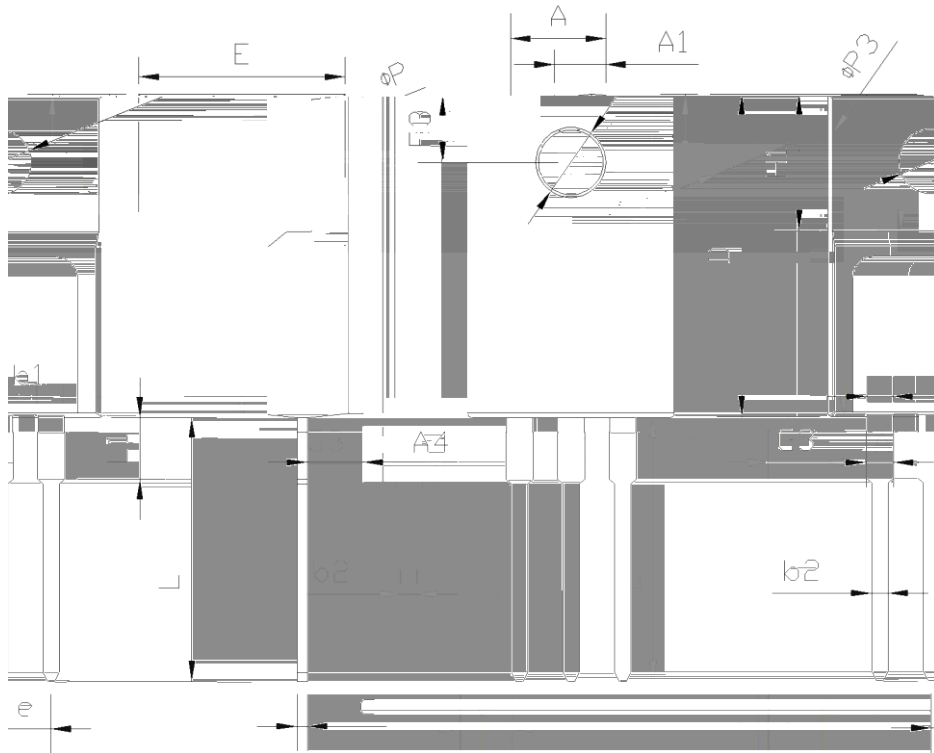


Figure 4. Diode reverse recovery test circuit & waveforms

Package Information



Symbol	mm		
	Min	Nom	Max
E	9.96	10.16	10.36
A	4.50	4.70	4.90
A1	2.34	2.54	2.74
A4	2.56	2.76	2.96
c	0.40	0.50	0.65
D	15.57	15.87	16.17
H1	6.70REF		
e	2.54BSC		
L	12.68	12.98	13.28
L1	2.88	3.03	3.18
K	3.03	3.18	3.38
K.	3.15	3.45	3.65
F3	3.15	3.30	3.45
G3	1.25	1.35	1.55
b1	1.18	1.28	1.43
b2	0.70	0.80	0.95

Version 1: TO220F-C package outline dimension

