

Absolute Maximum Ratings at $T_j=25^{\circ}\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	40	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾ , $T_C=25^{\circ}\text{C}$	I_D	200	A
Pulsed drain current ²⁾ , $T_C=25^{\circ}\text{C}$	$I_{D, pulse}$	600	A
Continuous diode forward current ¹⁾ , $T_C=25^{\circ}\text{C}$	I_S	200	A
Diode pulsed current ²⁾ , $T_C=25^{\circ}\text{C}$	$I_{S, Pulse}$	600	A
Power dissipation ³⁾ , $T_C=25^{\circ}\text{C}$	P_D	132	W
Single pulsed avalanche energy ⁵⁾	E_{AS}	200	mJ
Operation and storage temperature	T_{stg} T_j	-55 to 150	$^{\circ}\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	R_{JC}	0.95	$^{\circ}\text{C}/\text{W}$
Thermal resistance, junction-ambient ⁴⁾	R_{JA}	62	$^{\circ}\text{C}/\text{W}$

Electrical Characteristics at $T_j=25^{\circ}\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	40			V	$V_{GS}=0\text{ V}$, $I_D=250\ \mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	1.0		2.5	V	$V_{DS}=V_{GS}$, $I_D=250\ \mu\text{A}$
Drain-source on-state resistance	$R_{DS(ON)}$		1.25	1.50	m	$V_{GS}=10\text{ V}$, $I_D=55\text{ A}$
Drain-source on-state resistance	$R_{DS(ON)}$		2.0	3.0	m	$V_{GS}=6\text{ V}$, $I_D=55\text{ A}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20\text{ V}$
				-100		$V_{GS}=-20\text{ V}$
Drain-source leakage current	I_{DSS}			1	μA	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}					

Electrical Characteristics Diagrams

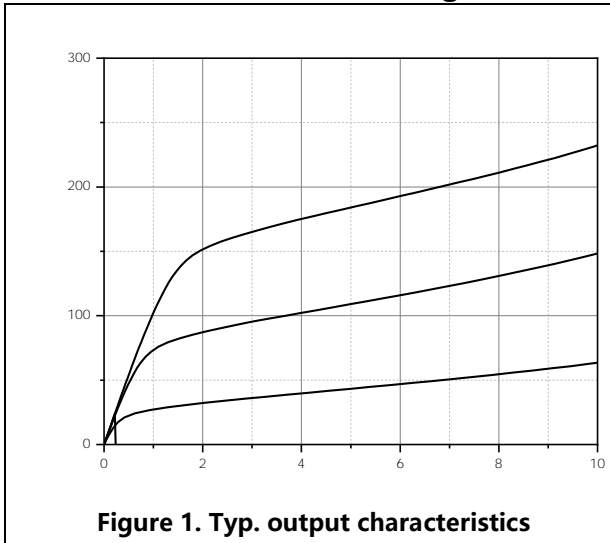


Figure 1. Typ. output characteristics

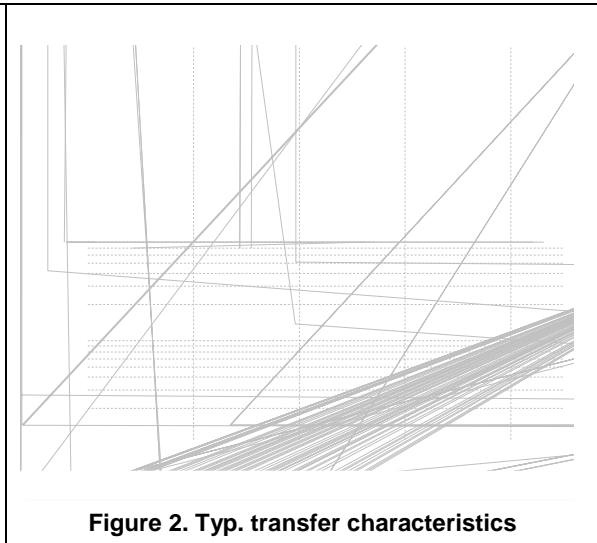


Figure 2. Typ. transfer characteristics

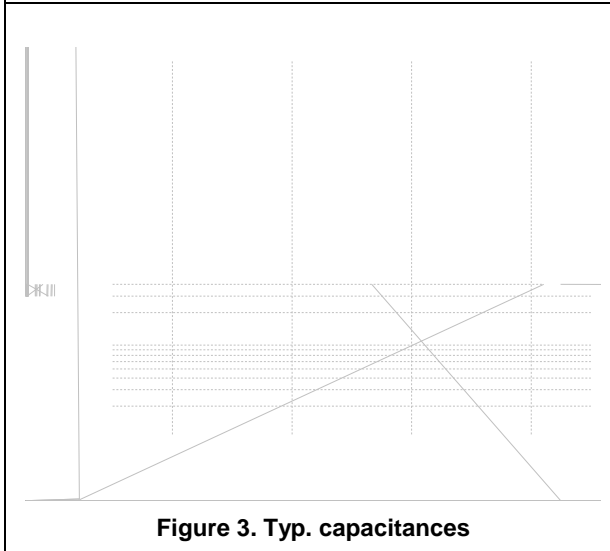


Figure 3. Typ. capacitances

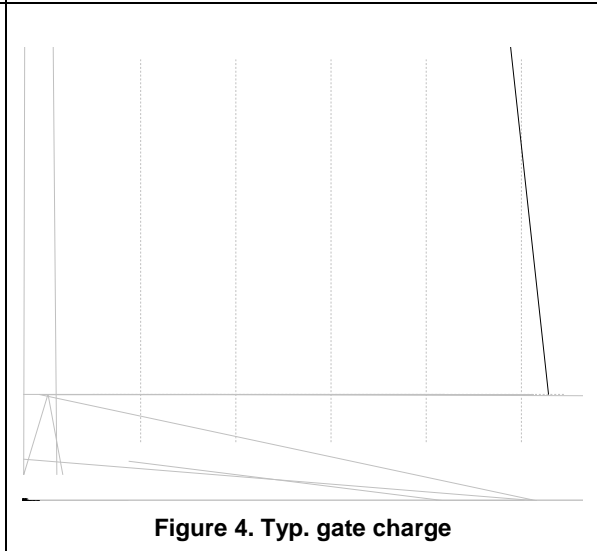


Figure 4. Typ. gate charge

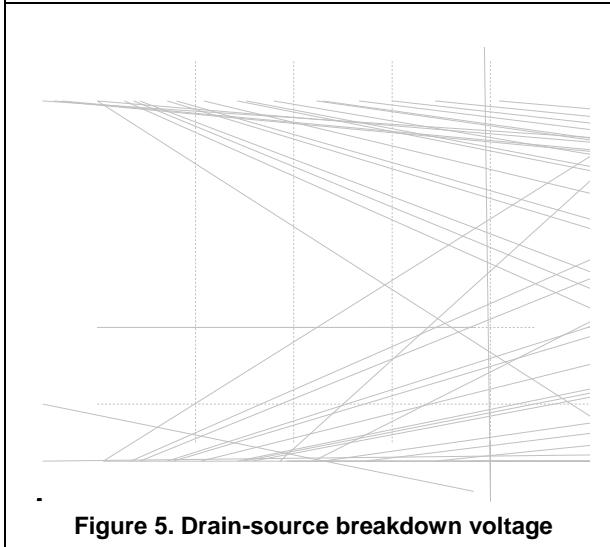


Figure 5. Drain-source breakdown voltage

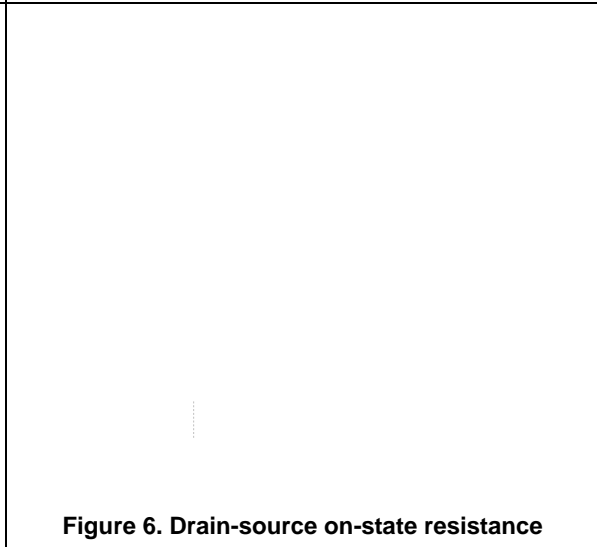
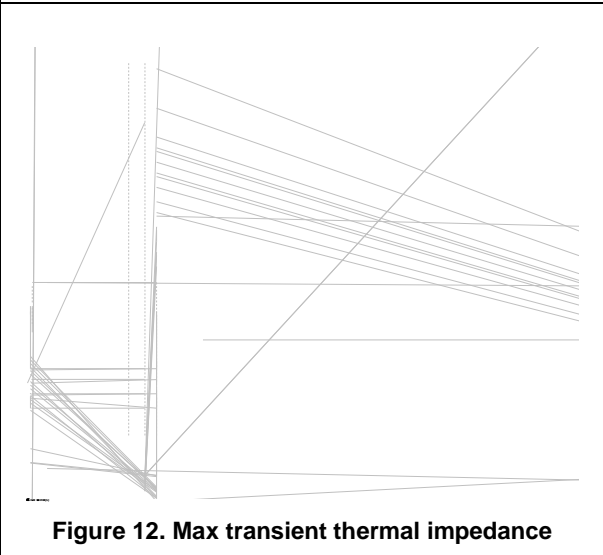
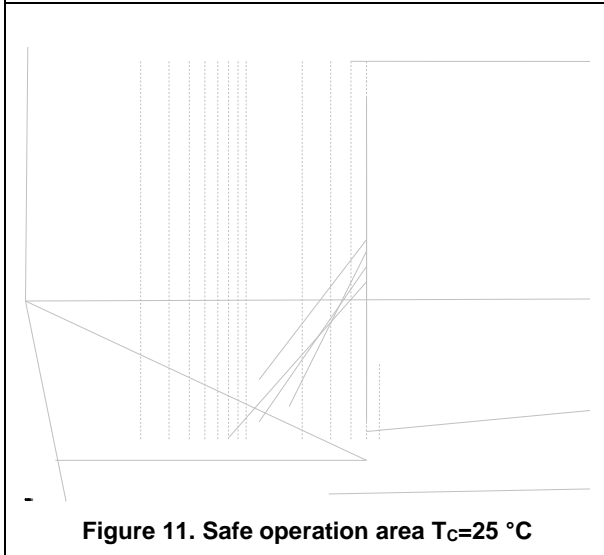
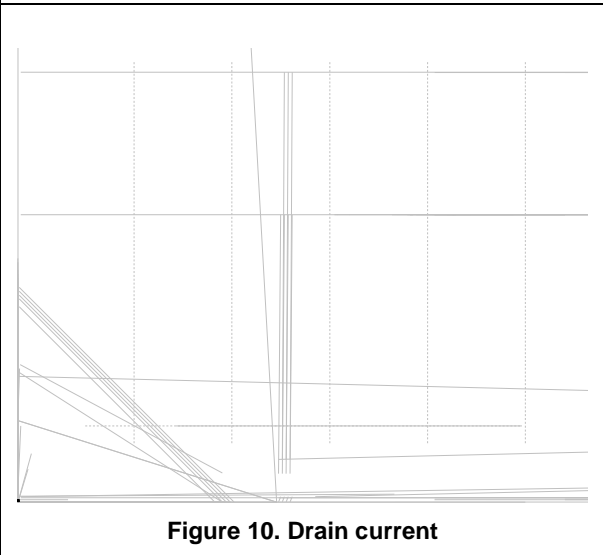
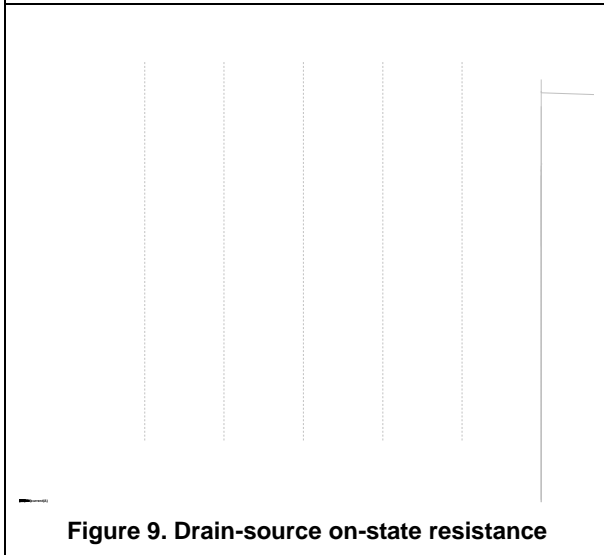
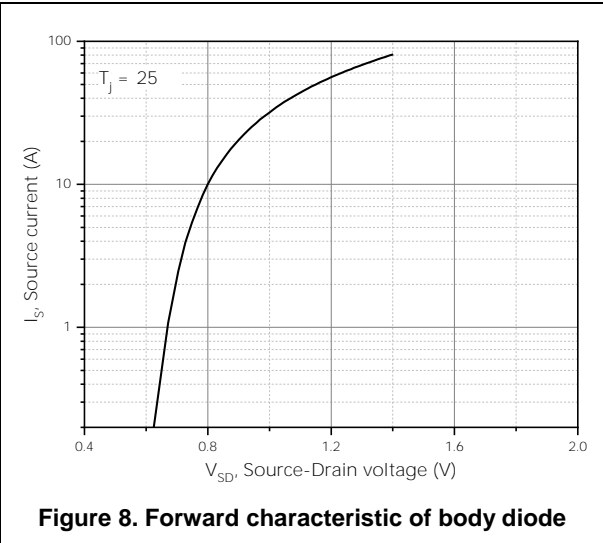
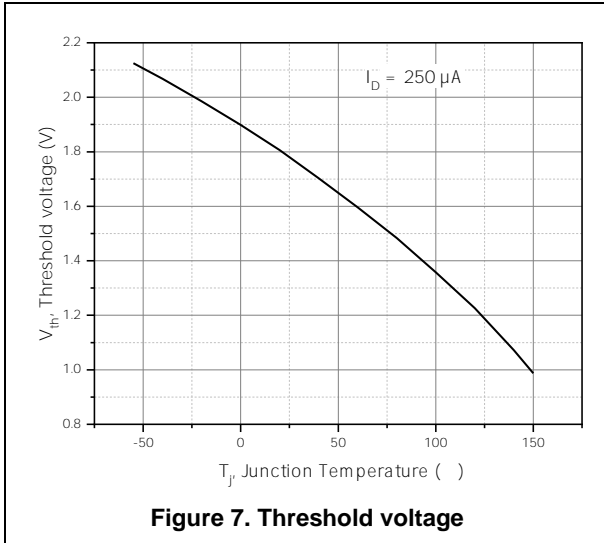


Figure 6. Drain-source on-state resistance



Test circuits and waveforms

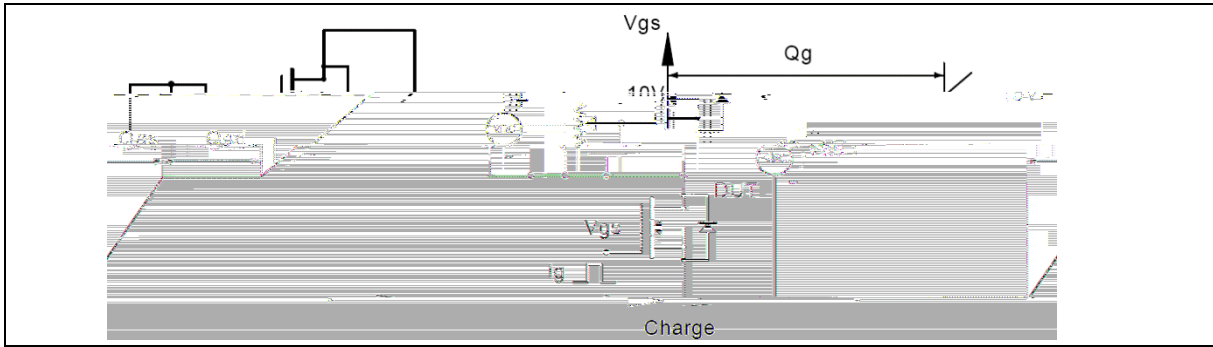


Figure 1. Gate charge test circuit & waveform

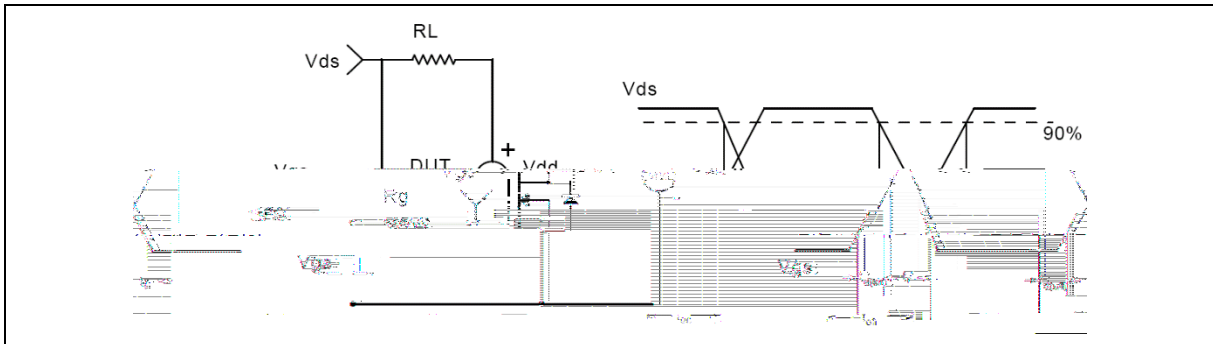


Figure 2. Switching time test circuit & waveforms

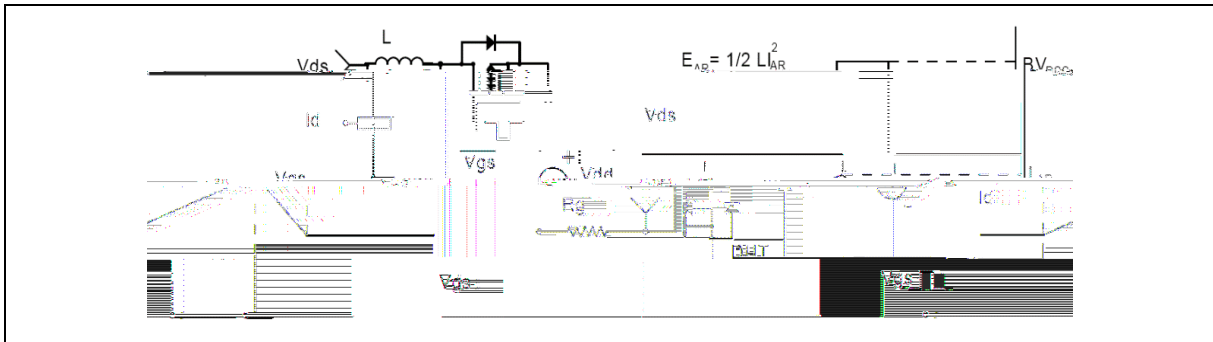


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

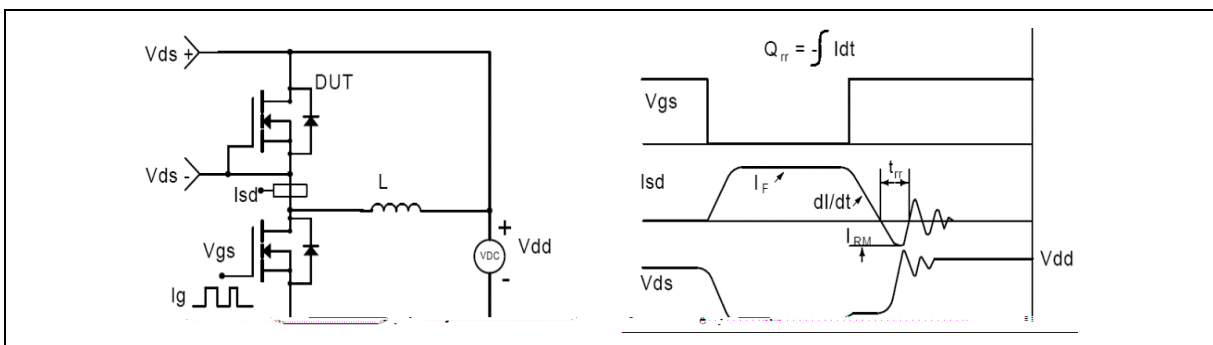
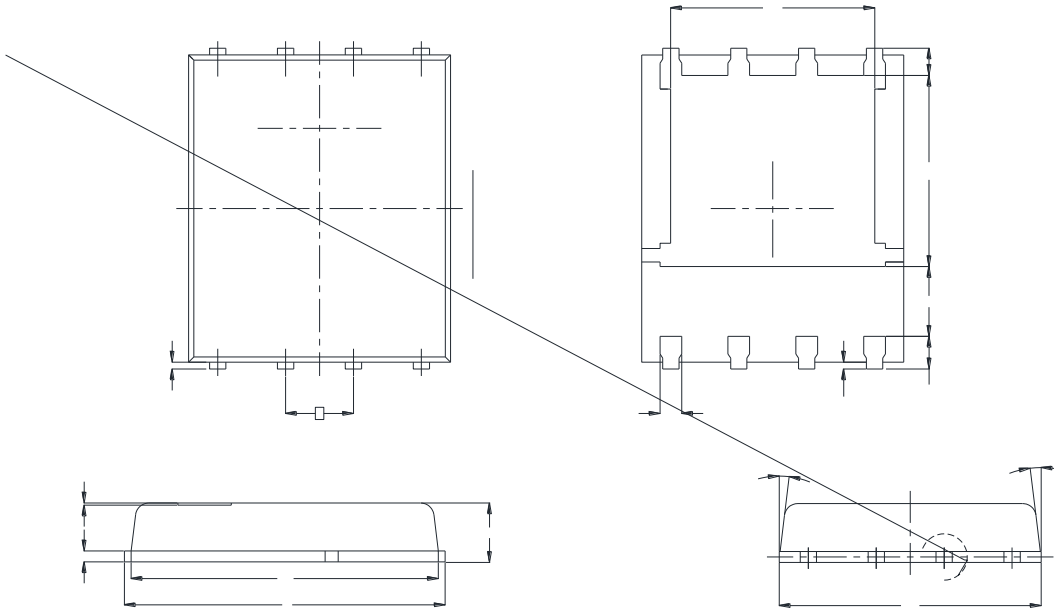


Figure 4. Diode reverse recovery test circuit & waveforms

Package Information



Symbol	mm		
	Min	Nom	Max
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
	0°	-	12°

Version 2: PDFN5*6-M package outline dimension

Ordering Information

Package Type	Units/ Reel	Reels / Inner Box	Units/ Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
PDFN5*6-P	5000	2	10000	5	50000
PDFN5*6-M	5000	2	10000	5	50000

Product Information

Product	Package	Pb Free	RoHS	Halogen Free
SFS04R02GF	PDFN5*6	yes	yes	yes

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Oriental Semiconductor hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

For further information on technology, delivery terms and conditions and prices, please contact the Oriental Semiconductor sales representatives (www.orientalsemi.com).

© Oriental Semiconductor Co.,Ltd. All Rights Reserved /