The GreenMOS® high voltage MOSFET utilizes charge balance technology to achieve outstanding low on-resistance and lower gate charge. It is engineered to minimize conduction loss, provide superior switching performance and robust avalanche capability.

GreenMOS®

RoHS compliant

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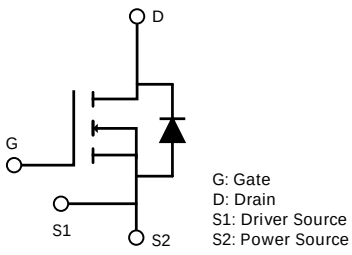
Parameter	Value	Unit
$V_{DS,\ min}$ @ $T_{j(max)}$	650	V
$I_{D,\ pulse}$	99	A
$R_{DS(ON),\ max}$ @ V_{GS}=10V	74	
Q_g	68.6	nC

Product Name	Package	Marking
OSG60R074JT3ZF	PDFN 8×8	OSG60R074JT3Z



Absolute Maximum Ratings at T_j=25 unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	600	V
Gate-source voltage	V_{GS}	±30	V
Continuous drain current[1], T_C=25 °C	I_D	33	A
Continuous drain current[1], T_C=100 °C		20.9	
Pulsed drain current[2], T_C=25 °C	$I_{D, pulse}$	99	A
Continuous diode forward current[1], T_C=25 °C	I_S	33	A
Diode pulsed current[2], T_C=25 °C	$I_{S, pulse}$	99	A
Power dissipation[3], T_C=25 °C	P_D	187	W
Single pulsed avalanche energy[5]	E_{AS}	640	mJ
MOSFET dv/dt ruggedness, V_{DS}	dv/dt	50	V/ns
Reverse diode dv/dt, V_{DS} SD D	dv/dt	50	V/ns
Operation and storage temperature	T_{stg}, T_j	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	R	0.67	°C/W
Thermal resistance, junction-ambient[4]	R	62	°C/W

Electrical Characteristics at T_j=25 unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	600			V	V_{GS}=0 V, I_D=1 mA
		650				V_{GS}=0 V, I_D=1 mA, T_j=150 °C
Gate threshold voltage	$V_{GS(th)}$	3.0		5.0	V	V_{DS}=V_{GS}, I_D=1 mA
Drain-source on-state resistance	$R_{DS(ON)}$		60	74	m	V_{GS}=10 V, I_D=15.1 A
			146			V_{GS}=10 V, I_D=15.1 A, T_j=150 °C
Gate-source leakage current	I_{GSS}			100	nA	V_{GS}=30 V
				-100		V_{GS}=-30 V
Drain-source leakage current	I_{DSS}			10	A	V_{DS}=600 V, V_{GS}=0 V
Gate resistance	R_G		8.8			

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		3340		pF	V_{GS}=0 V, V_{DS}=50 V, 100 kHz
Output capacitance	C_{oss}		177		pF	
Reverse transfer capacitance	C_{rss}		4.1		pF	
Effective output capacitance, energy related	$C_{o(er)}$		112		pF	V_{GS}=0 V, V_{DS}=0 V-400 V
Effective output capacitance, time related	$C_{o(tr)}$		662		pF	
Turn-on delay time	$t_{d(on)}$		31		ns	V_{GS}=10 V, V_{DS}=400 V, R_G I_D=20 A
Rise time	t_r		44.2		ns	
Turn-off delay time	$t_{d(off)}$		88		ns	
Fall time	t_f		26.2		ns	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q_g		68.6		nC	V_{GS}=10 V, V_{DS}=400 V, I_D=20 A
Gate-source charge	Q_{gs}		22.1		nC	
Gate-drain charge	Q_{gd}		22.7		nC	
Gate plateau voltage	$V_{plateau}$		6.8		V	

Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward voltage	V_{SD}			1.3	V	I_S=33 A, V_{GS}=0 V
Reverse recovery time	t_{rr}		156		ns	V_R=400 V, I_S=20 A, di/dt=10
Reverse recovery charge	Q_{rr}		0.9		uC	
Peak reverse recovery current	I_{rrm}		11.3		A	

Note

1) Calculated continuous current based on maximum allowable junction temperature.
2) Repetitive rating; pulse width limited by max. junction temperature.
3) Pd is based on max. junction temperature, using junction-case thermal resistance.
4) The value of R is measured with the device mounted on 1 in square FR-4 board with 2oz. Copper, in a still air environment with T_a=25 °C.
5) V_{DD}=100 V, V_{GS}=10 V, L=80 mH, starting T_j=25 °C.

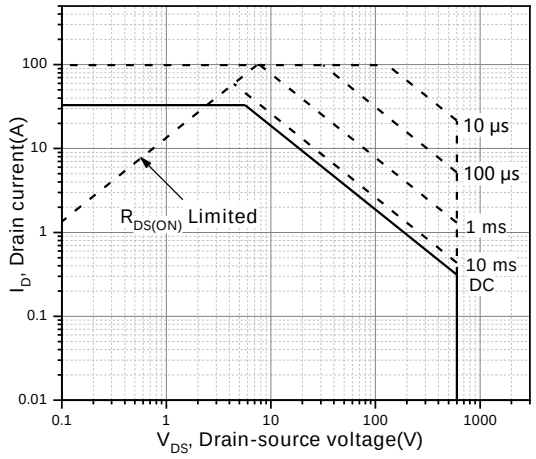


Figure 13. Safe operation area T_C=25 °C

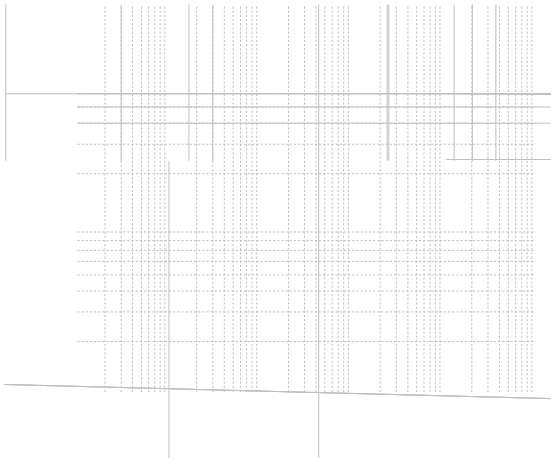


Figure 14. Max. transient thermal impedance

Test circuits and waveforms

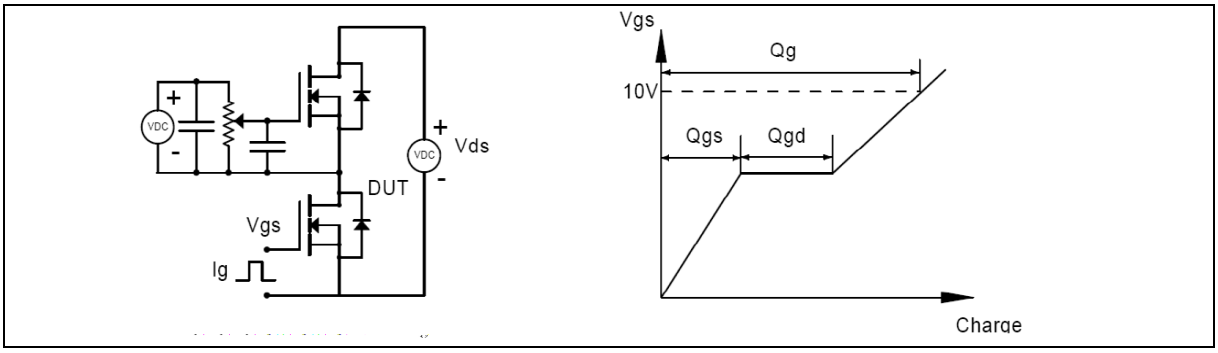


Figure 1. Gate charge test circuit & waveform

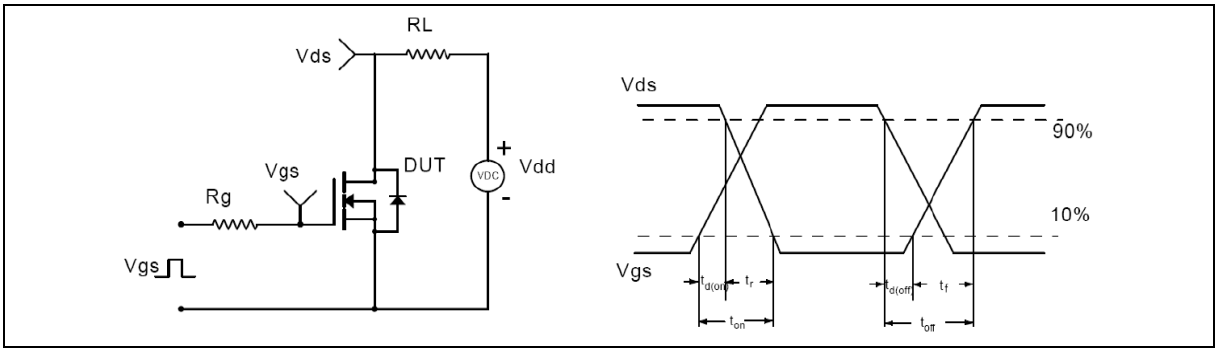


Figure 2. Switching time test circuit & waveforms

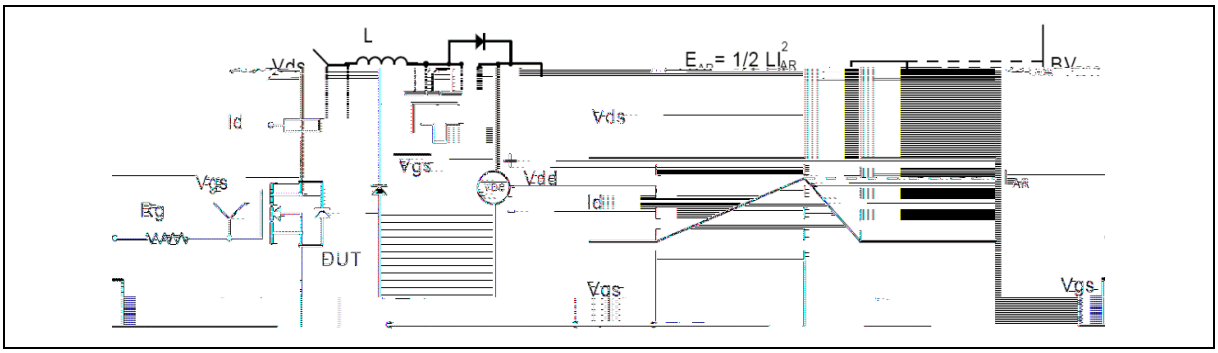


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

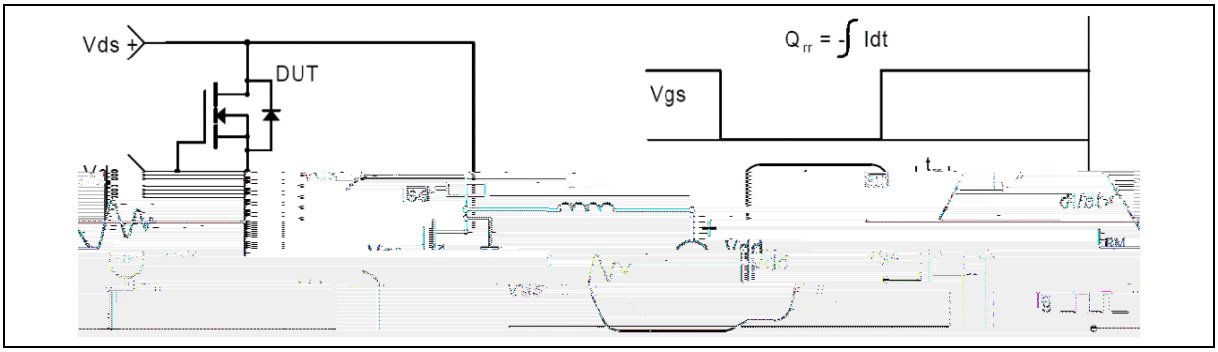
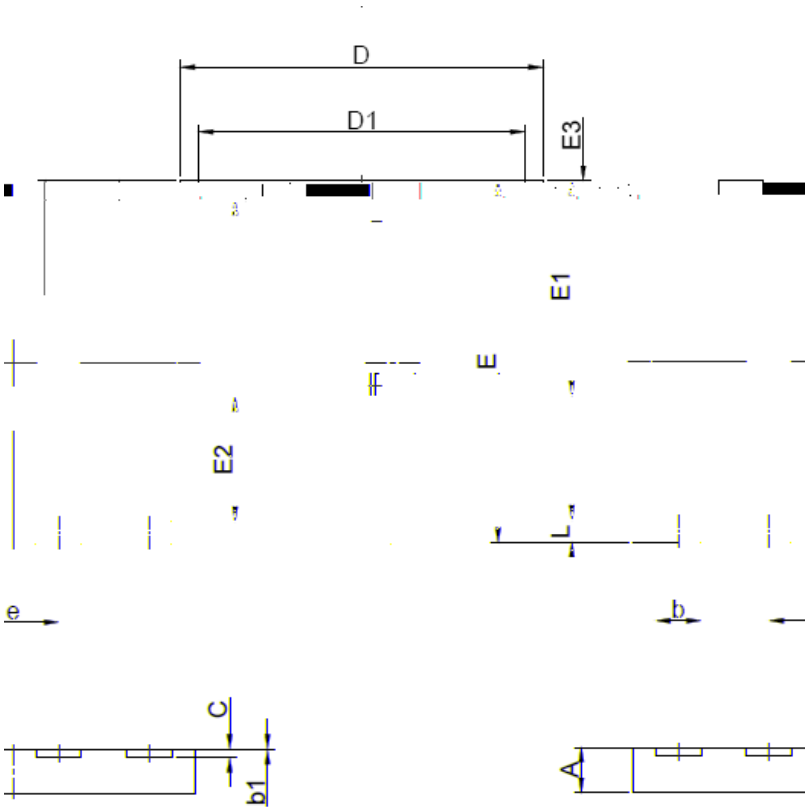


Figure 4. Diode reverse recovery test circuit & waveforms

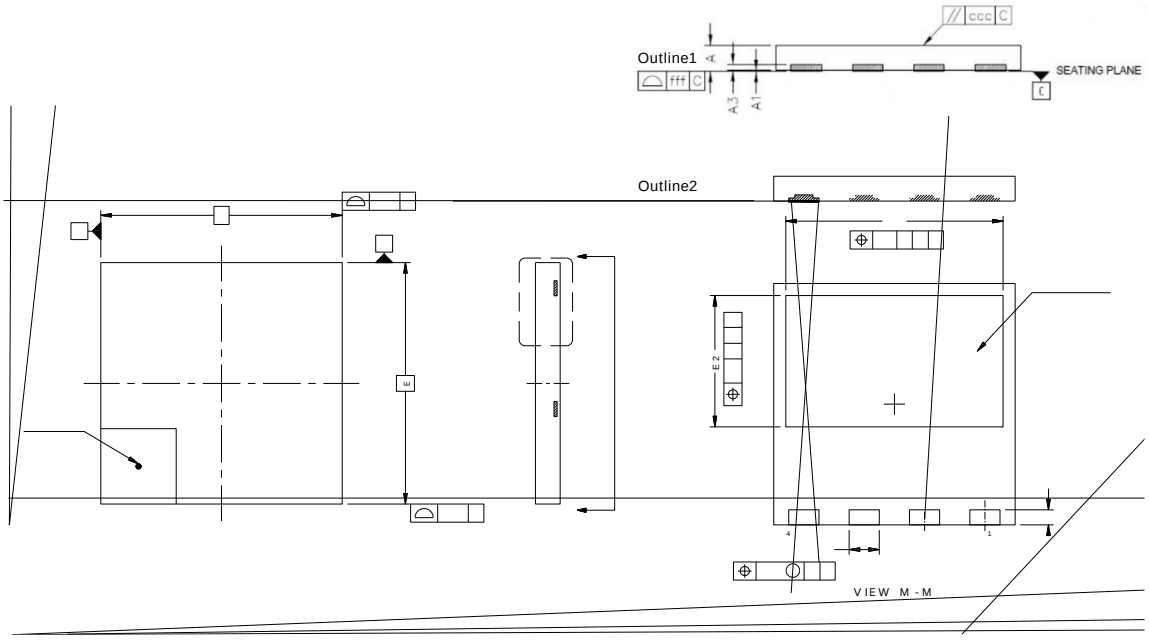
Package Information



Symbol	mm		
	Min	Nom	Max
A	0.90	1.00	1.10
b	0.90	1.00	1.10
b1	0.00	0.02	0.05
C	0.2 REF		
D	7.90	8.00	8.10
D1	7.10	7.20	7.30
E	7.90	8.00	8.10
E1	4.65	4.75	4.85
E2	2.65	2.75	2.85
E3	0.3	0.4	0.5
e	2.0 BSC		
L	0.4	0.5	0.6

Version 1: PDFN 8×8-L package outline dimension

Package Information



Symbol	mm	
	Min	Max
A	0.75	0.95
A1	0.00	0.05
A3	0.10	0.30
b	0.90	1.10
D	7.90	8.10
E	7.90	8.10
D2	7.10	7.30
E1	2.65	2.85
E2	4.25	4.45
e	2.0 BSC	
L	0.40	0.60
aaa	0.1	
ggg	0.05	
ccc	0.05	
fff	0.05	

Version 2: PDFN 8×8-S package outline dimension