

GENERAL DESCRIPTION

The GreenMOS[®] high voltage MOSFET utilizes charge balance technology to achieve outstanding low on-resistance and lower gate charge. It is engineered to minimize conduction loss, provide superior switching performance and robust avalanche capability.

The GreenMOS[®] Generic series is optimized for extreme switching performance to minimize switching loss. It is tailored for high power density applications to meet the highest efficiency standards.

FEATURES

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APPLICATIONS

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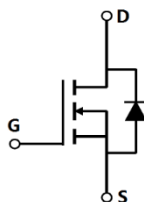
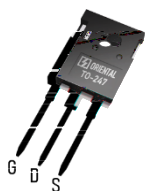
KEY PERFORMANCE PARAMETERS

Parameter	Value	Unit
$V_{DS, min} @ T_{j(max)}$	700	V
$I_{D, pulse}$	60	A
$R_{DS(ON), max} @ V_{GS}=10V$	200	
Q_g	24.8	nC

MARKING INFORMATION

Product Name	Package	Marking
OSG65R200HF	TO247	OSG65R200H

PACKAGE PIN INFORMATION



Absolute Maximum Ratings at $T_j=25$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	650	V
Gate-source voltage	V_{GS}	± 30	V
Continuous drain current ¹⁾ , $T_C=25$ °C	I_D	20	A
Continuous drain current ¹⁾ , $T_C=100$ °C		12.5	
Pulsed drain current ²⁾ , $T_C=25$ °C	$I_{D, pulse}$	60	A
Continuous diode forward current ¹⁾ , $T_C=25$ °C	I_S	20	A
Diode pulsed current ²⁾ , $T_C=25$ °C	$I_{S, pulse}$	60	A
Power dissipation ³⁾ , $T_C=25$ °C	P_D	151	W
Single pulsed avalanche energy ⁵⁾	E_{AS}	600	mJ
MOSFET dv/dt ruggedness, V_{DS}	dv/dt	50	V/ns
Reverse diode dv/dt, V_{DS}	dv/dt	15	V/ns
Operation and storage temperature	T_{stg}, T_j	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	R	0.82	°C/W
Thermal resistance, junction-ambient ⁴⁾	R	62	°C/W

Electrical Characteristics at $T_j=25$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	650			V	$V_{GS}=0$ V, $I_D=250$ uA
		700	774			$V_{GS}=0$ V, $I_D=250$ u A, $T_j=150$ °C
Gate threshold voltage	$V_{GS(th)}$	2.0		4.0	V	$V_{DS}=V_{GS}$, $I_D=250$ u A
Drain-source on-state resistance	$R_{DS(ON)}$		0.16	0.2		$V_{GS}=10$ V, $I_D=10$ A
			0.42			$V_{GS}=10$ V, $I_D=10$ A, $T_j=150$ °C
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=30$ V
				-100		$V_{GS}=-30$ V
Drain-source leakage current	I_{DSS}			1	A	$V_{DS}=650$ V, $V_{GS}=0$ V

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		1433		pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, 00 kHz
Output capacitance	C_{oss}		92.5		pF	
Reverse transfer capacitance	C_{rss}		3.9		pF	
Turn-on delay time	$t_{d(on)}$		40.1		ns	$V_{GS}=10\text{ V}$, $V_{DS}=520\text{ V}$, $R_G=25$ $I_D=20\text{ A}$
Rise time	t_r		49.8		ns	
Turn-off delay time	$t_{d(off)}$		57.3		ns	
Fall time	t_f		63.7		ns	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q_g		24.8		nC	$V_{GS}=10\text{ V}$, $V_{DS}=520\text{ V}$, $I_D=20\text{ A}$
Gate-source charge	Q_{gs}		7.2		nC	
Gate-drain charge	Q_{gd}		8.2		nC	
Gate plateau voltage	$V_{plateau}$		5.6		V	

Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward voltage	V_{SD}			1.4	V	$I_S=20\text{ A}$, $V_{GS}=0\text{ V}$
Reverse recovery time	t_{rr}		380		ns	$I_S=20\text{ A}$,
Reverse recovery charge	Q_{rr}		5.3			

Electrical Characteristics Diagrams

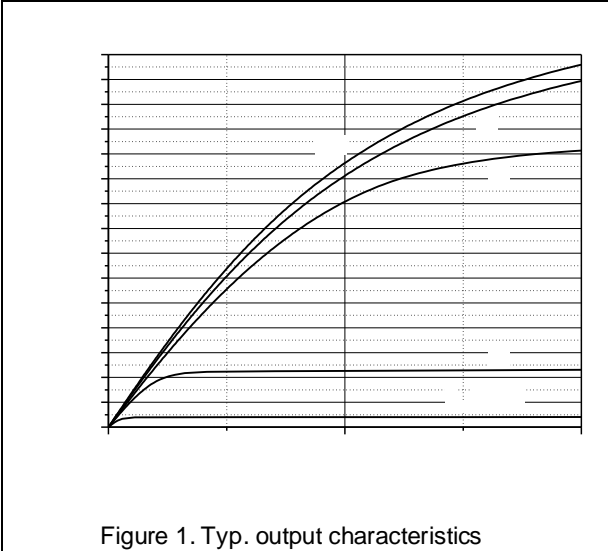


Figure 1. Typ. output characteristics

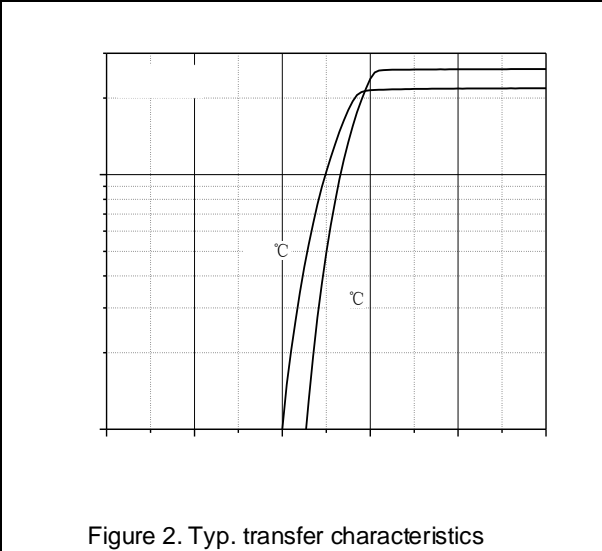


Figure 2. Typ. transfer characteristics

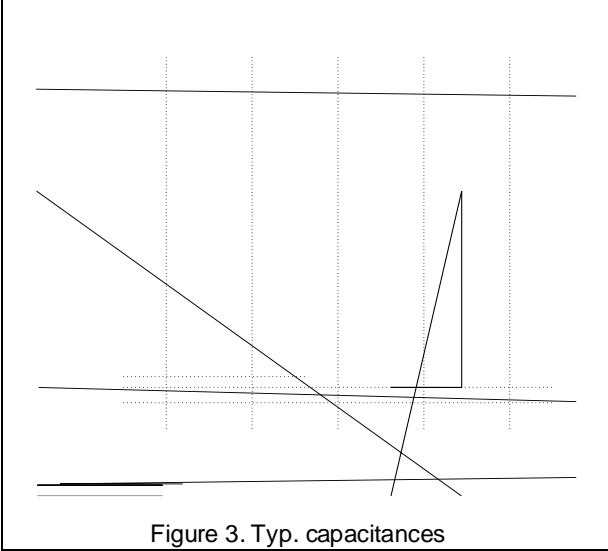


Figure 3. Typ. capacitances

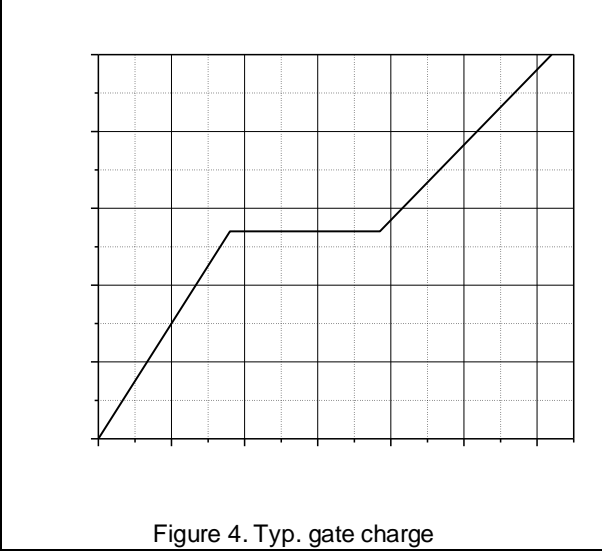


Figure 4. Typ. gate charge

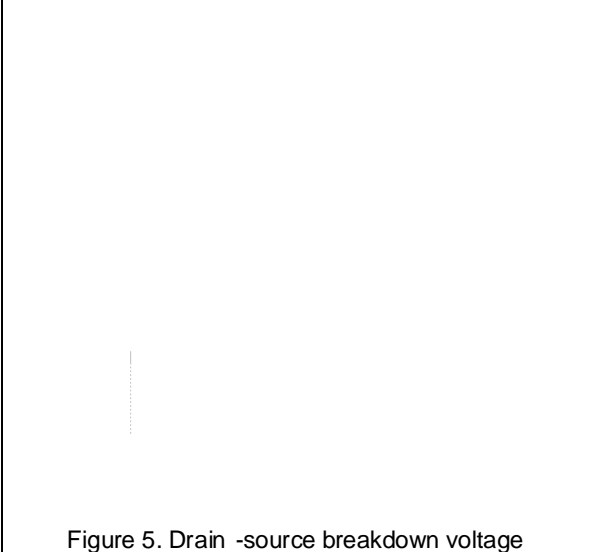


Figure 5. Drain -source breakdown voltage

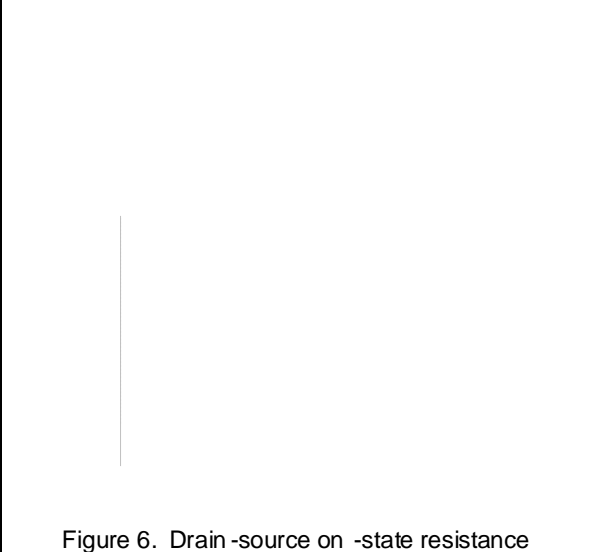


Figure 6. Drain -source on -state resistance

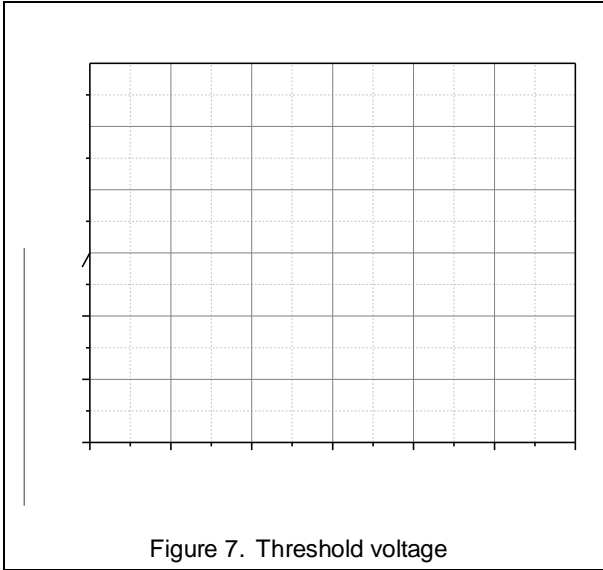


Figure 7. Threshold voltage

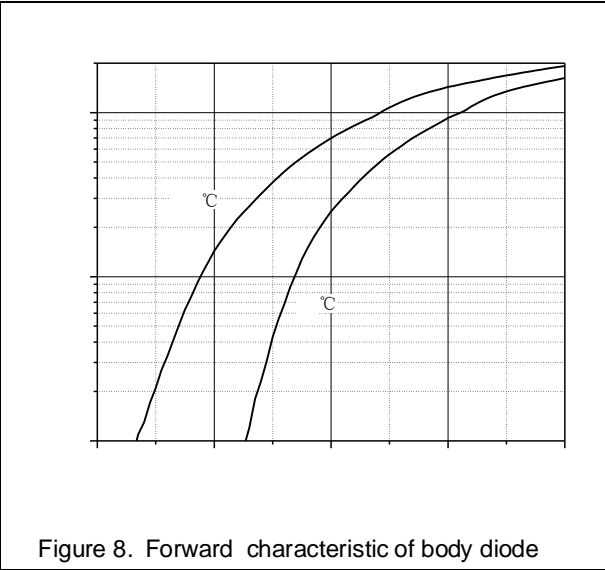


Figure 8. Forward characteristic of body diode

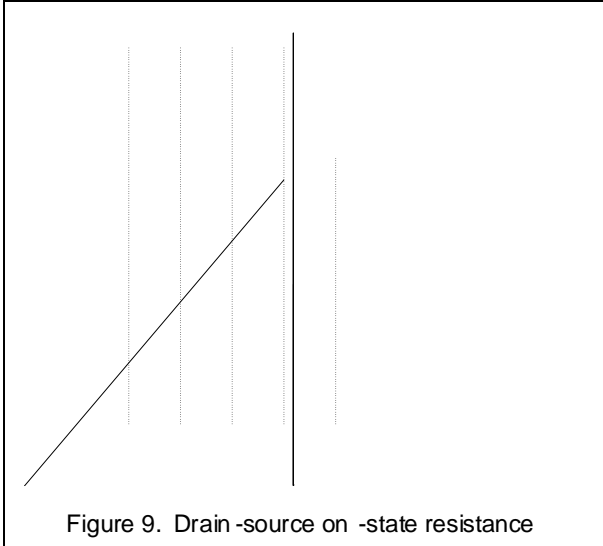


Figure 9. Drain-source on-state resistance

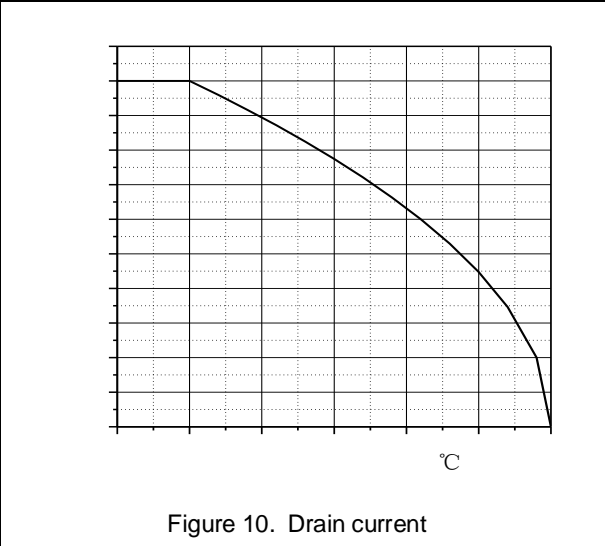


Figure 10. Drain current

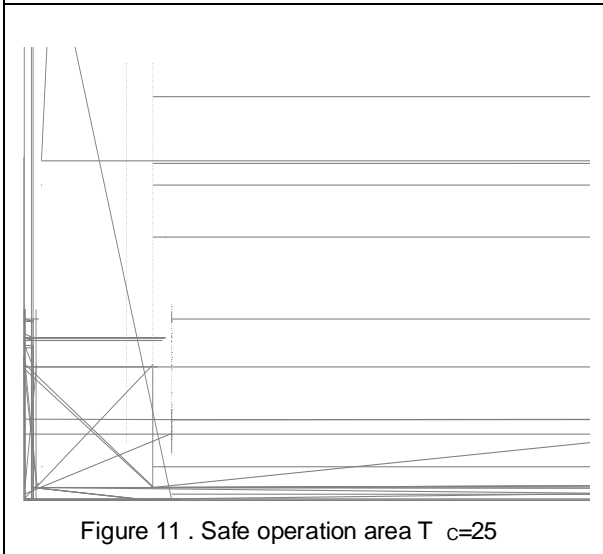


Figure 11. Safe operation area $T_c=25$

Test circuits and waveforms

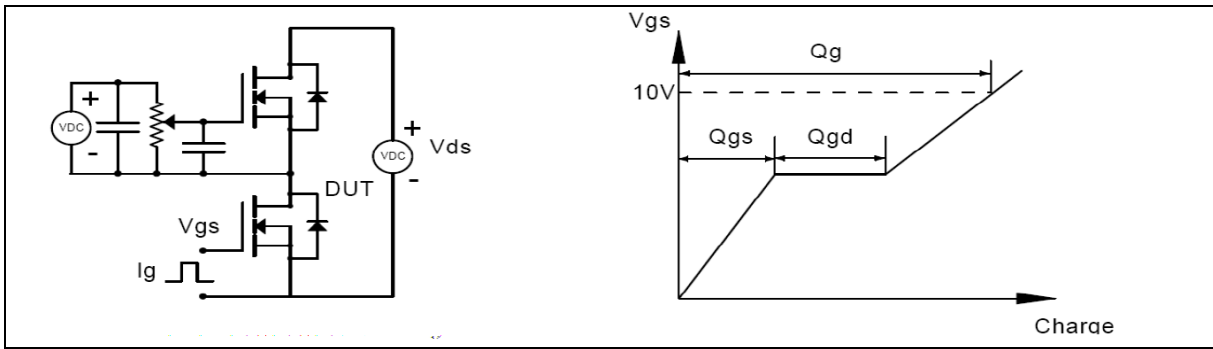


Figure 1. Gate charge test circuit & waveform

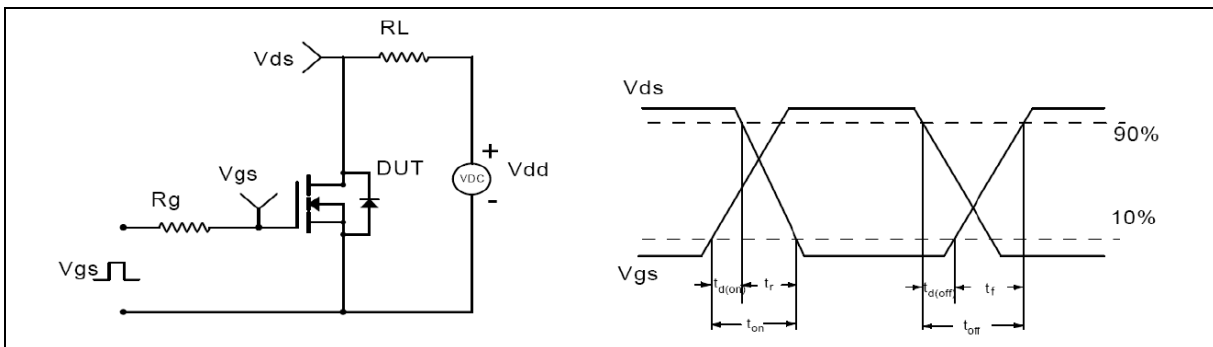


Figure 2. Switching time test circuit & waveforms

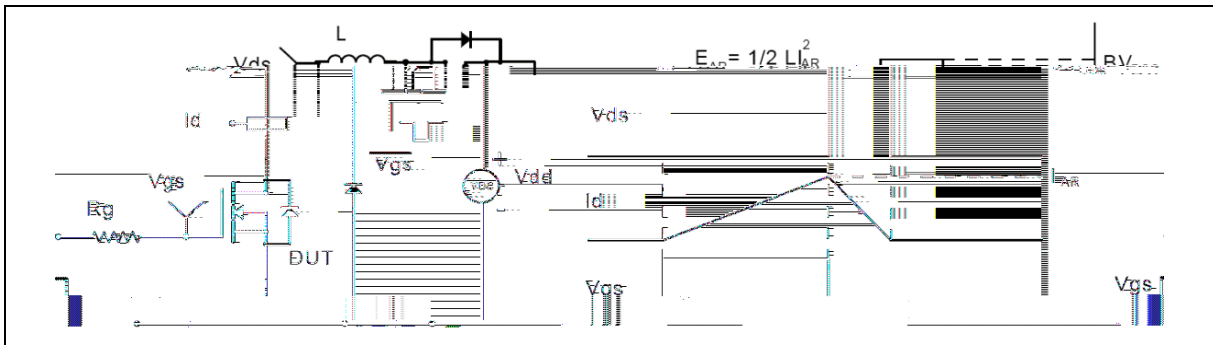
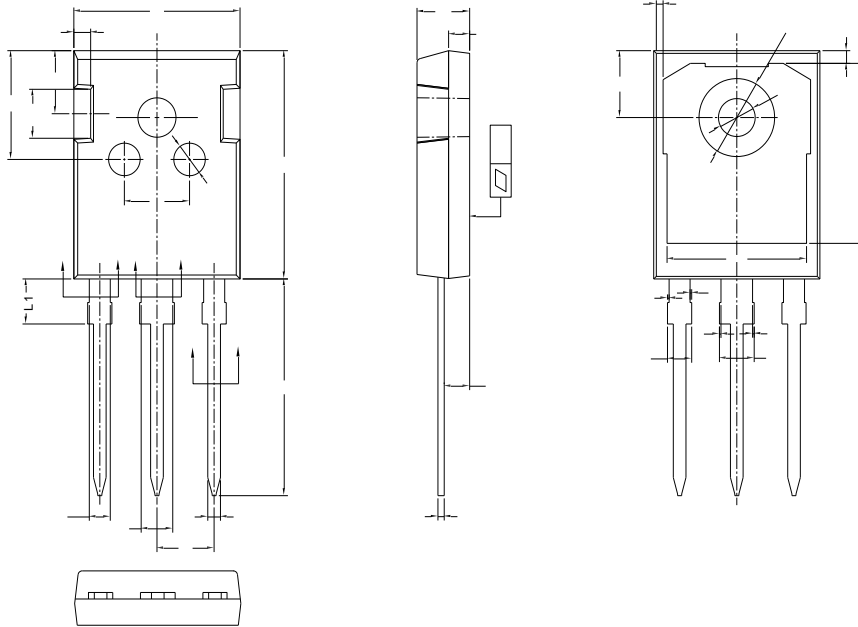


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms



Figure 4. Diode reverse recovery test circuit & waveforms

Package Information



Symbol	mm		
	Min	Nom	Max
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
a	0.00	-	0.15
a [*]	0.00	-	0.15
b	1.16	-	1.26
b2	1.96	-	2.06
b4	2.96	-	3.06
b6	-	-	2.25
b7	-	-	3.25
c	0.59	-	0.66
c1	0.58	0.60	0.62
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.17	1.35
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.40	4.50	4.60
E3	1.50	1.60	1.70
e	5.436 BSC		
L	19.80	19.92	20.10
L1	-	-	4.30
M	0.35	-	0.95
P	3.40	3.50	3.60
P1	7.00	-	7.40
P2	2.40	2.5	2.6
Q	5.60	-	6.0
S	6.05	6.15	6.25
T	9.8	-	10.20
U	6.00	-	6.40

Version1: TO247-J package outline dimension

Package Information

Symbol	mm
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