The GreenMOS® high voltage MOSFET utilizes charge balance technology to achieve outstanding low on-resistance and lower gate charge. It is engineered to minimize conduction loss, provide superior switching performance and robust avalanche capability.

The GreenMOS® Generic series is optimized for extreme switching performance to minimize switching loss. It is tailored for high power density applications to meet the highest efficiency standards.

GreenMOS®

RoHS compliant

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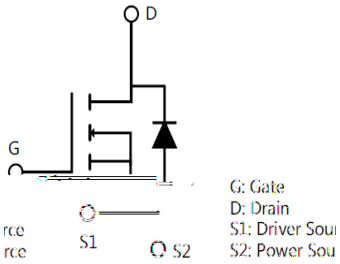
| Parameter | Value | Unit |
|---|---|---|
| $V_{DS,\ min}$ @ $T_{j(max)}$ | 700 | V |
| $I_{D,\ pulse}$ | 60 | A |
| $R_{DS(ON)\ ,\ max}$ @ $V_{GS}$=10V | 200 | |
| $Q_g$ | 24 | nC |

| Product Name | Package | Marking |
|---|---|---|
| OSG65R200JT3F | PDFN 8×8 | OSG65R200JT3 |

vise noted

| | Symbol | Value | Unit |
|---|---|---|---|
| | $V_{DS}$ | 650 | V |
| | $V_{GS}$ | ±30 | V |
| | $I_D$ | 20 | A |
| Continuous drain current[1], $T_C$=100 °C | | 12.6 | |
| Pulsed drain current[2], $T_C$=25 °C | $I_{D,\ pulse}$ | 60 | A |

## Dynamic Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test condition |
|---|---|---|---|---|---|---|
| Input capacitance | $C_{iss}$ | | 842 | | pF | $V_{GS}$=0 V, $V_{DS}$=50 V, Hz |
| Output capacitance | $C_{oss}$ | | 58 | | pF | |
| Reverse transfer capacitance | $C_{rss}$ | | 2.5 | | pF | |
| Effective output capacitance, energy related | $C_{o(er)}$ | | 40 | | pF | $V_{GS}$ =0 V, $V_{DS}$ =0 V-400 V |
| Effective output capacitance, time related | $C_{o(tr)}$ | | 226 | | pF | |

## Electrical Characteristics Diagrams

**Figure 1. Typ. output characteristics**

**Figure 2. Typ. transfer characteristics**

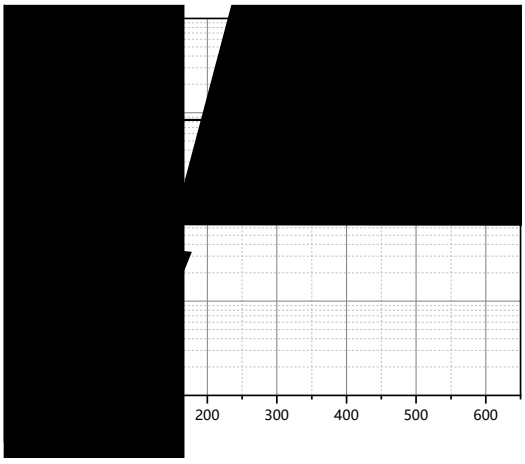



**Figure 3. Typ. capacitances**

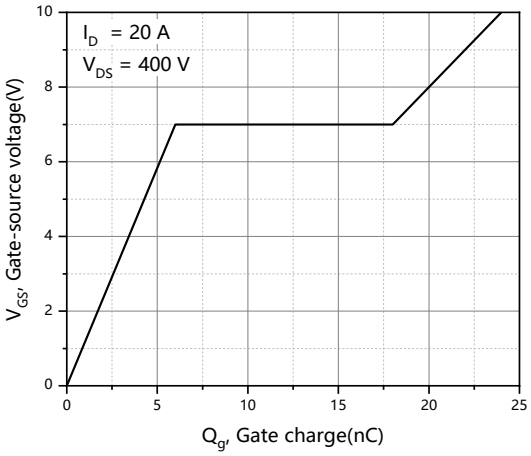



**Figure 4. Typ. gate charge**

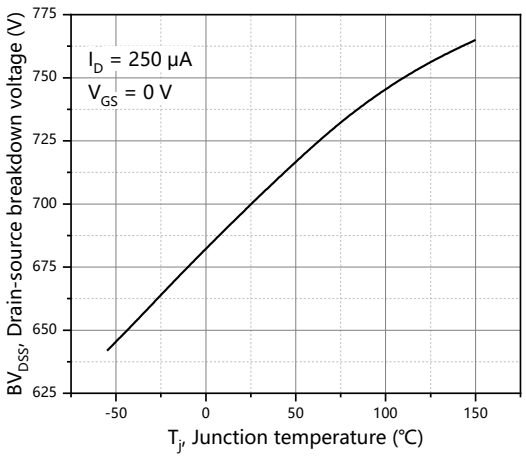



**Figure 5. Drain-source breakdown voltage**

**Figure 6. Drain-source on-state resistance**

Figure 7. Threshold voltage

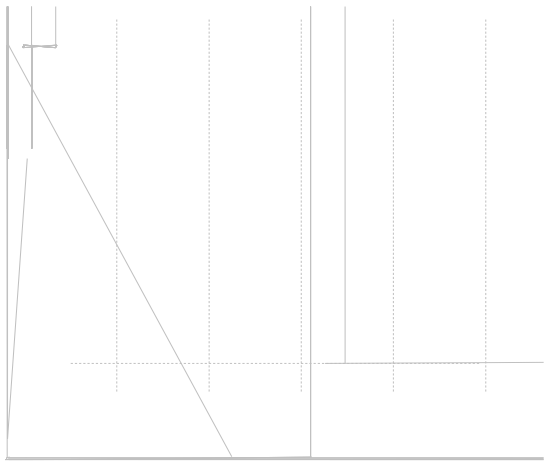


Figure 8. Forward characteristic of body diode

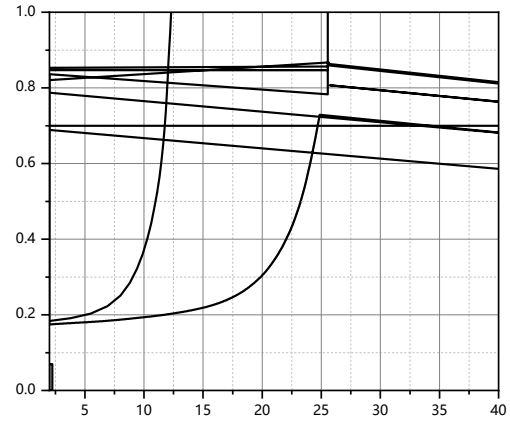



Figure 9. Drain-source on-state resistance

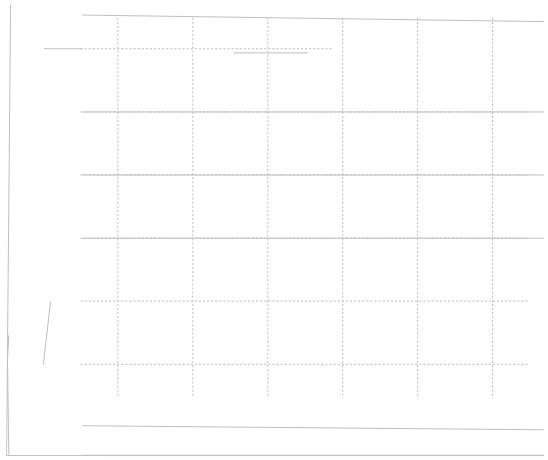


Figure 10. Drain current

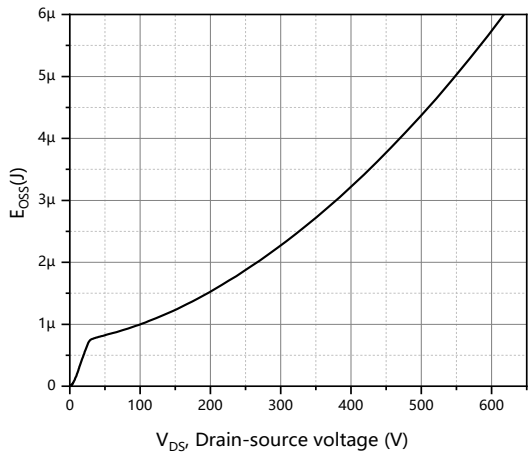



Figure 11. Typ. Coss stored energy

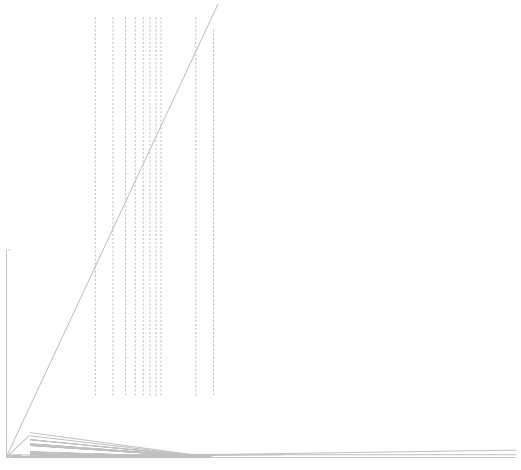


Figure 12. Safe operation area for $T_C$=25

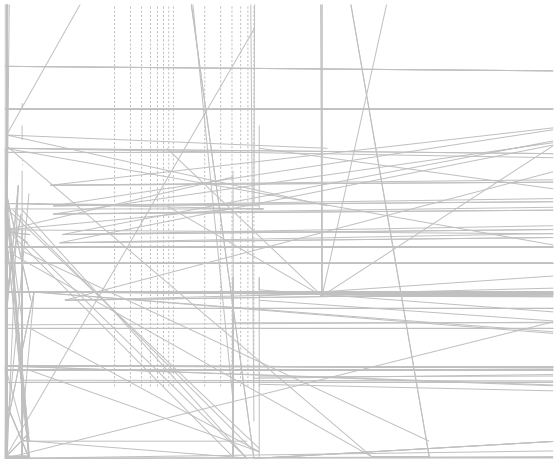


**Figure 13. Max transient thermal impedance**

## Test circuits and waveforms

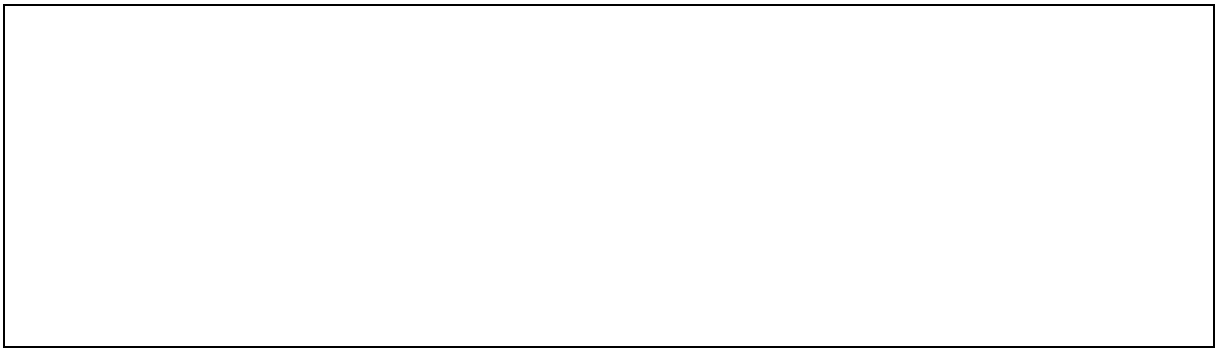


**Figure 1. Gate charge test circuit & waveform**

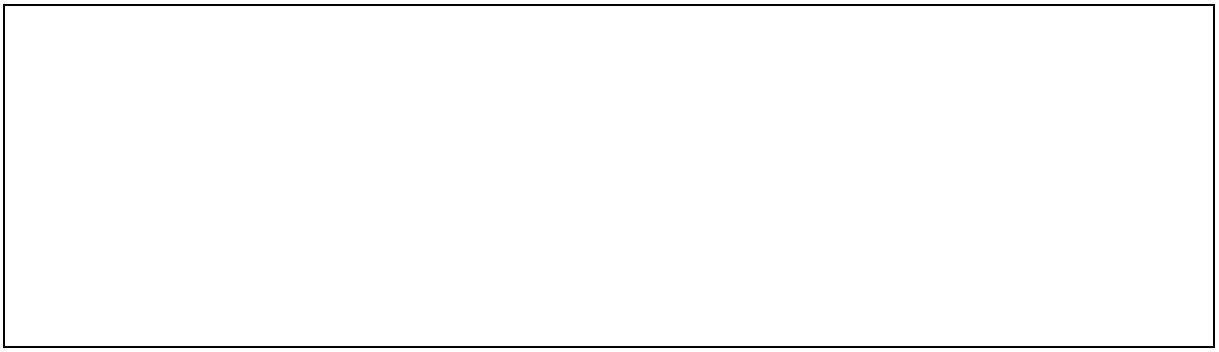


**Figure 2. Switching time test circuit & waveforms**

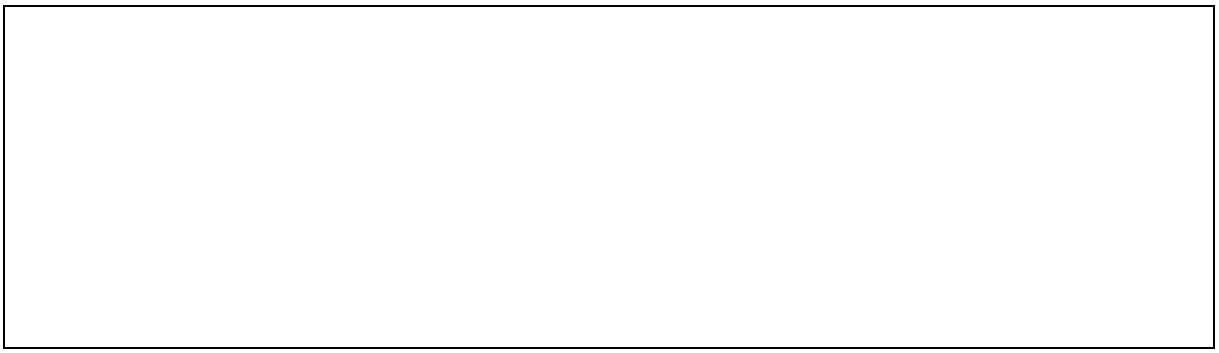


**Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms**

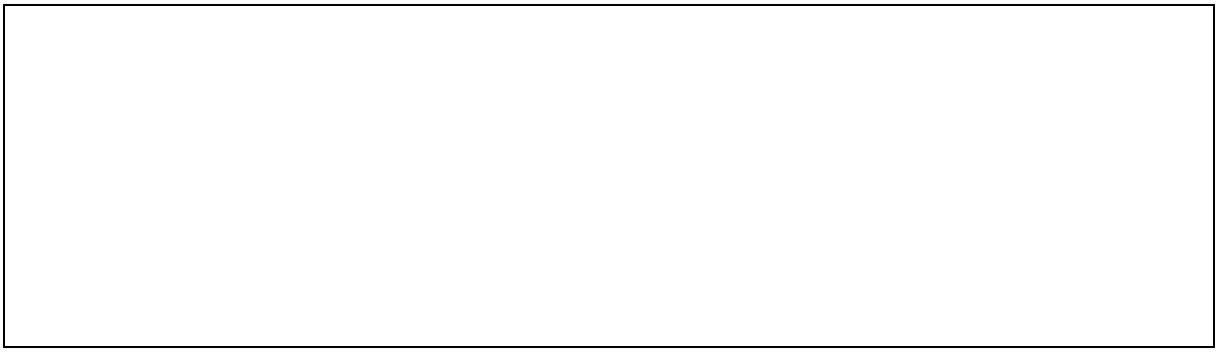
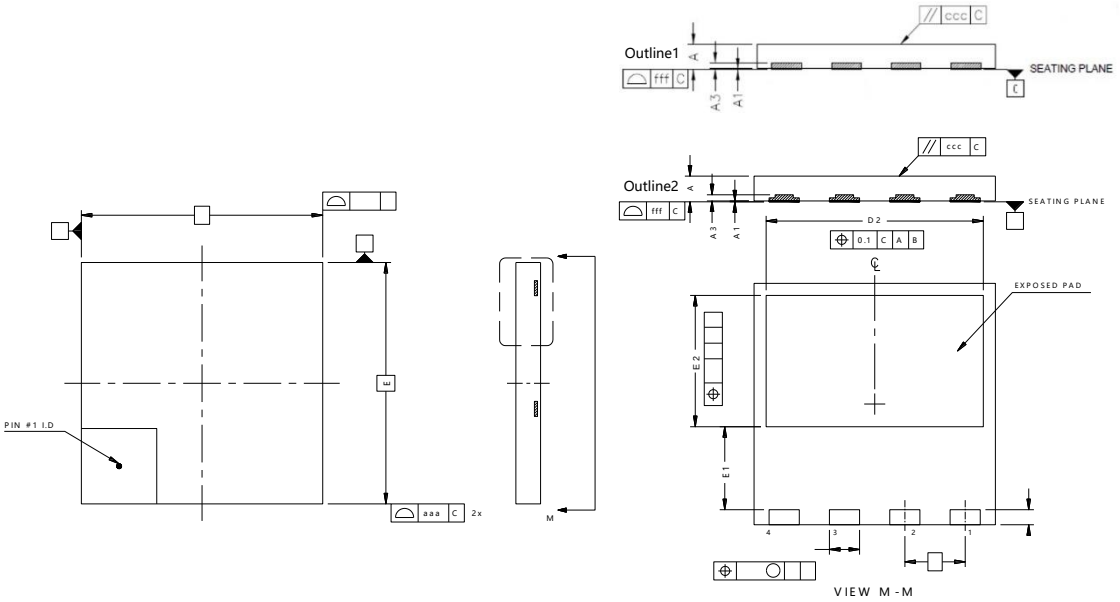


**Figure 4. Diode reverse recovery test circuit & waveforms**

## Package Information




| Symbol | mm | |
|---|---|---|
| | Min | Max |
| A | 0.75 | 0.95 |
| A1 | 0.00 | 0.05 |
| A3 | 0.10 | 0.30 |
| b | 0.90 | 1.10 |
| D | 7.90 | 8.10 |
| E | 7.90 | 8.10 |
| D2 | 7.10 | 7.30 |
| E1 | 2.65 | 2.85 |
| E2 | 4.25 | 4.45 |
| e | 2.0 BSC | |
| L | 0.40 | 0.60 |
| aaa | 0.1 | |
| ggg | 0.05 | |
| ccc | 0.05 | |
| fff | 0.05 | |

Version 1: PDFN8×8-S package outline dimension