

The GreenMOS<sup>®</sup> high voltage MOSFET utilizes charge balance technology to achieve outstanding low on-resistance and lower gate charge. It is engineered to minimize conduction loss, provide superior switching performance and robust avalanche capability.

The GreenMOS<sup>®</sup> Generic series is optimized for extreme switching performance to minimize switching loss. It is tailored for high power density applications to meet the highest efficiency standards.

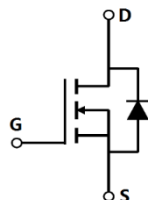
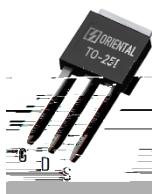
GreenMOS<sup>®</sup>



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Parameter	Value	Unit
$V_{DS, min} @ T_{j(max)}$	700	V
$I_{D, pulse}$	9	A
$R_{DS(ON), max} @ V_{GS}=10V$	2	
$Q_g$	6.3	nC

Product Name	Package	Marking
OSG65R2KAF	TO251	OSG65R2KA



**Absolute Maximum Ratings** at  $T_j=25$  unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-source voltage	$V_{DS}$	650	V
Gate-source voltage	$V_{GS}$	$\pm 30$	V
Continuous drain current <sup>1)</sup> , $T_C=25$ °C	$I_D$	3	A
Continuous drain current <sup>1)</sup> , $T_C=100$ °C		1.9	
Pulsed drain current <sup>2)</sup> , $T_C=25$ °C	$I_{D, pulse}$	9	A
Continuous diode forward current <sup>1)</sup> , $T_C=25$ °C	$I_S$	3	A
Diode pulsed current <sup>2)</sup> , $T_C=25$ °C	$I_{S, pulse}$	9	A
Power dissipation <sup>3)</sup> , $T_C=25$ °C	$P_D$	22.3	W
Single pulsed avalanche energy <sup>5)</sup>	$E_{AS}$	70	mJ
MOSFET dv/dt ruggedness, $V_{DS}$	dv/dt	50	V/ns
Reverse diode dv/dt, $V_{DS}$	dv/dt	15	V/ns
Operation and storage temperature	$T_{stg}, T_j$	-55 to 150	°C

**Thermal Characteristics**

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	R	5.6	°C/W
Thermal resistance, junction-ambient <sup>4)</sup>	R	62	°C/W

**Electrical Characteristics** at  $T_j=25$  unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	$BV_{DSS}$	650			V	$V_{GS}=0$ V, $I_D=250$ A
		700	780			$V_{GS}=0$ V, $I_D$ , $T_j=150$ °C
Gate threshold voltage	$V_{GS(th)}$	2.0		4.0	V	$V_{DS}=V_{GS}$ , $I_D=250$ A
Drain-source on-state resistance	$R_{DS(on)}$		1.7	2		$V_{GS}=10$ V, $I_D=1$ A
			4.1			$V_{GS}=10$ V, $I_D=1$ A, $T_j=150$ °C
Gate-source leakage current	$I_{GSS}$			100	nA	$V_{GS}=30$ V
				-100		$V_{GS}=-30$ V
Drain-source leakage current	$I_{DSS}$			1	A	$V_{DS}=650$ V, $V_{GS}=0$ V

### Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	$C_{iss}$		172		pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , Hz
Output capacitance	$C_{oss}$		13.7		pF	
Reverse transfer capacitance	$C_{rss}$		0.84		pF	
Turn-on delay time	$t_{d(on)}$		20.7		ns	$V_{GS}=10\text{ V}$ , $V_{DS}=400\text{ V}$ , $R_G=50$ $I_D=3\text{ A}$
Rise time	$t_r$		11.4		ns	
Turn-off delay time	$t_{d(off)}$		65.6		ns	
Fall time	$t_f$		29.6		ns	

### Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	$Q_g$		6.3		nC	$V_{GS}=10\text{ V}$ , $V_{DS}=400\text{ V}$ , $I_D=3\text{ A}$
Gate-source charge	$Q_{gs}$		1.2		nC	
Gate-drain charge	$Q_{gd}$		3.3		nC	
Gate plateau voltage	$V_{plateau}$		5.6		V	

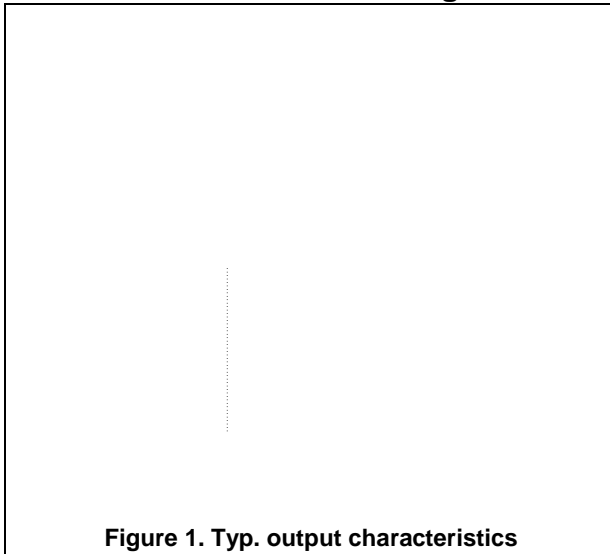
### Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward voltage	$V_{SD}$			1.3	V	$I_S=3\text{ A}$ , $V_{GS}=0\text{ V}$
Reverse recovery time	$t_{rr}$		138.4		ns	$I_S=3\text{ A}$ ,
Reverse recovery charge	$Q_{rr}$		0.7		C	
Peak reverse recovery current	$I_{rrm}$		8.58		A	

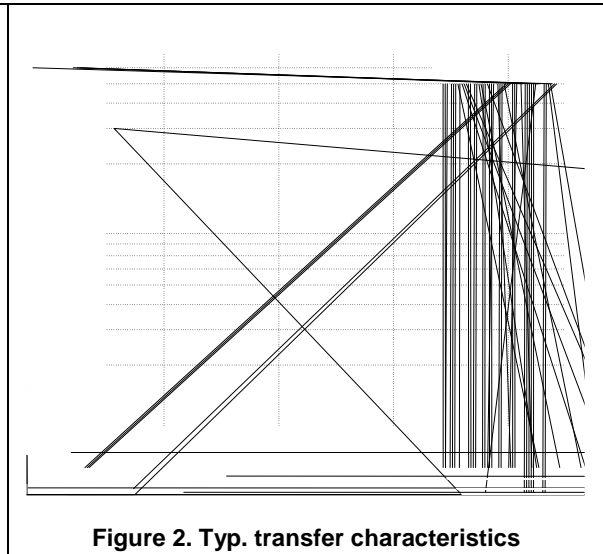
### Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3)  $P_d$  is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of  $R_{\theta}$  is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_a=25\text{ °C}$ .
- 5)  $V_{DD}=50\text{ V}$ ,  $V_{GS}=10\text{ V}$ ,  $L=22.5\text{ mH}$ , starting  $T_j=25\text{ °C}$ .

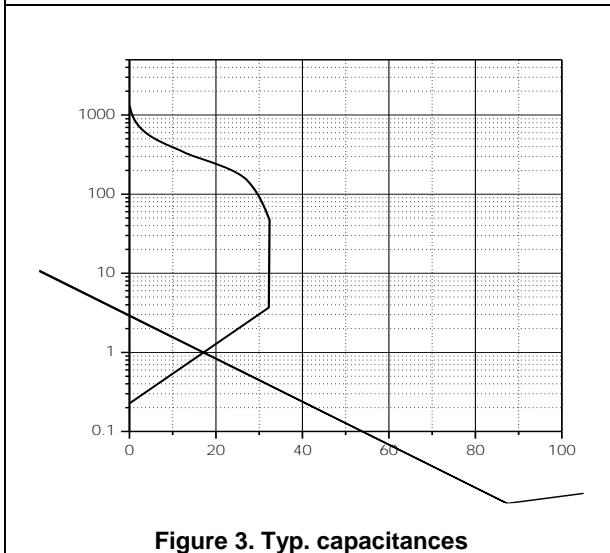
**Electrical Characteristics Diagrams**



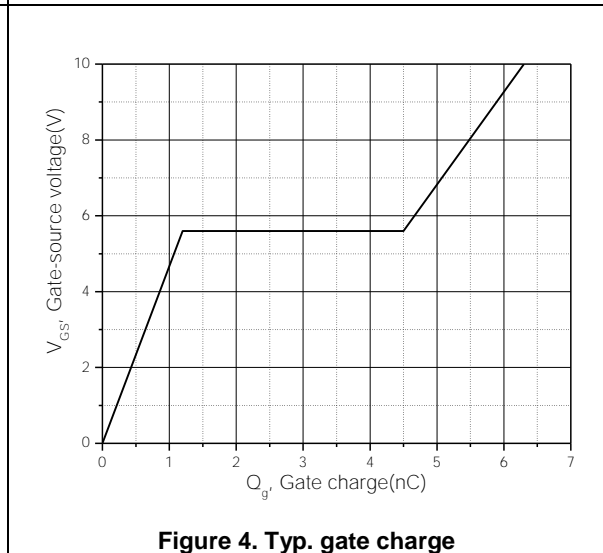
**Figure 1. Typ. output characteristics**



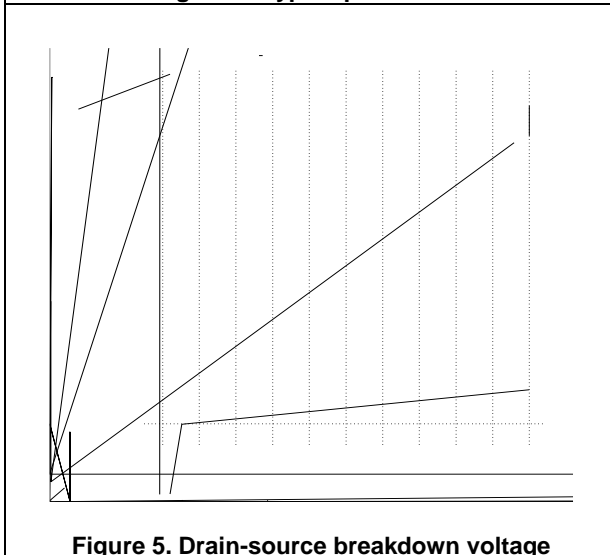
**Figure 2. Typ. transfer characteristics**



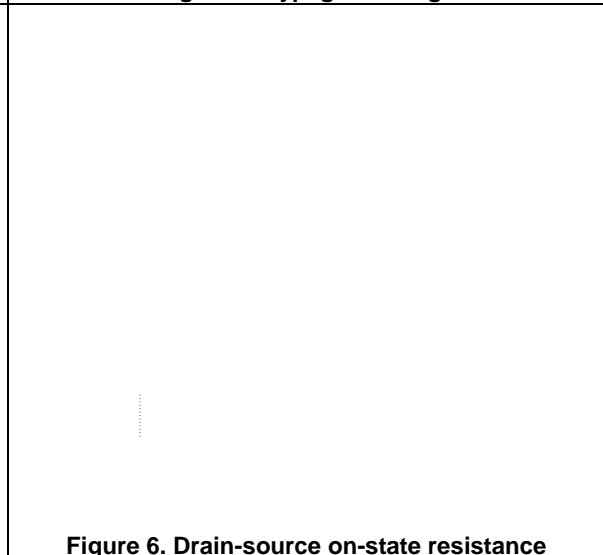
**Figure 3. Typ. capacitances**



**Figure 4. Typ. gate charge**



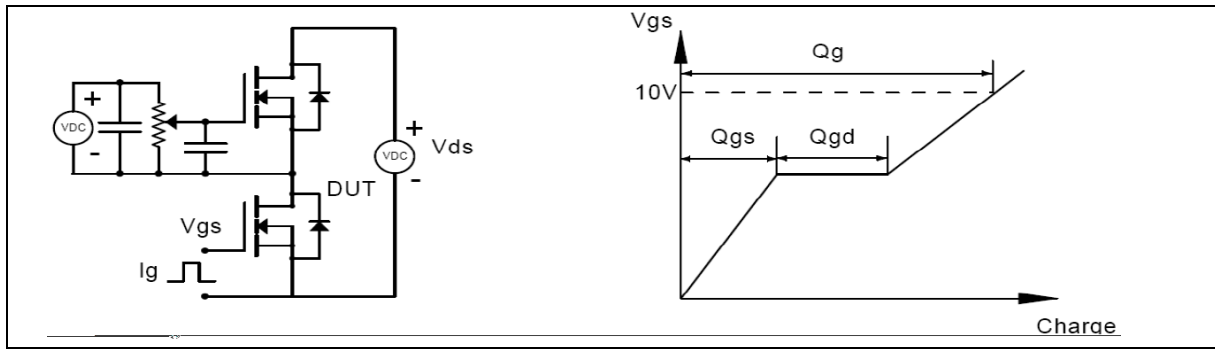
**Figure 5. Drain-source breakdown voltage**



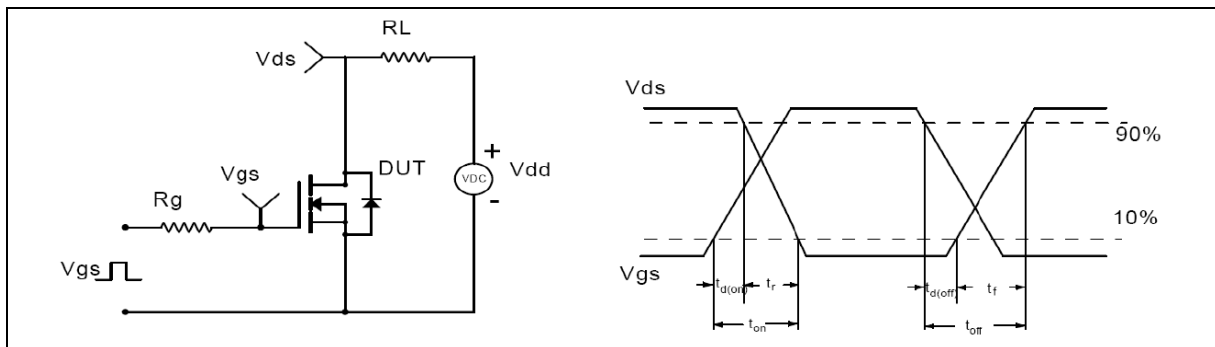
**Figure 6. Drain-source on-state resistance**

Enhancement Mode N-

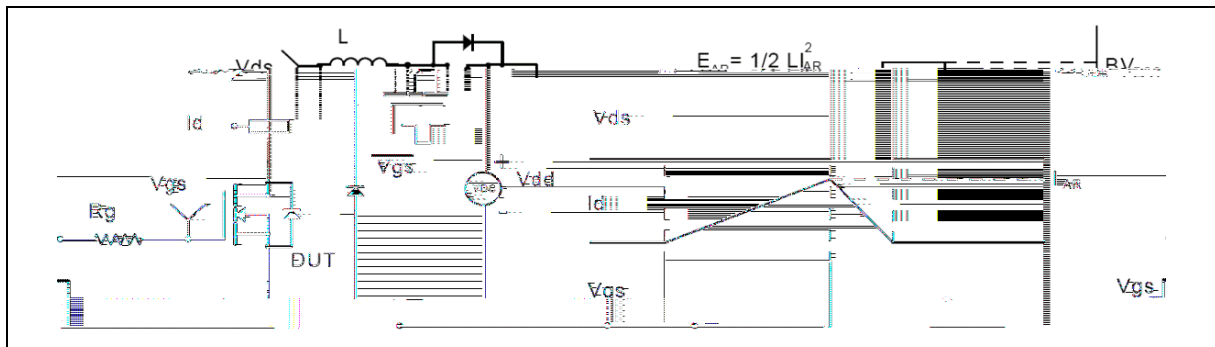
**Test circuits and waveforms**



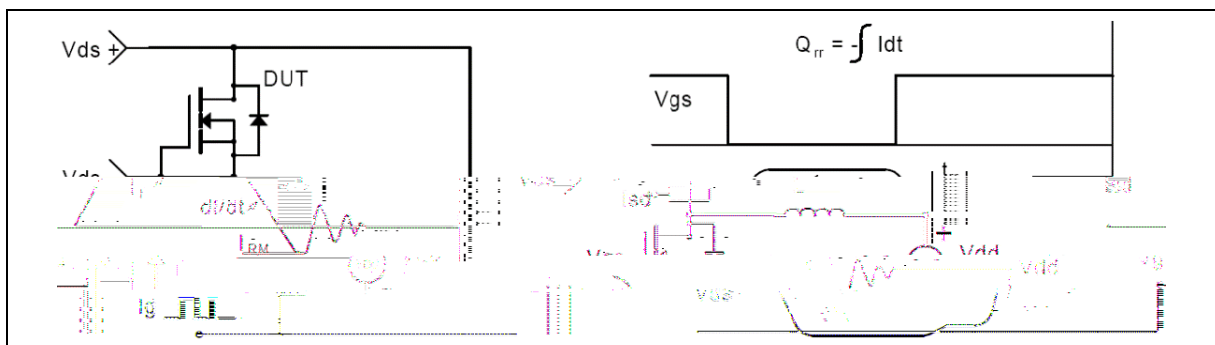
**Figure 1. Gate charge test circuit & waveform**



**Figure 2. Switching time test circuit & waveforms**



**Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms**



**Figure 4. Diode reverse recovery test circuit & waveforms**

## Package Information

Symbol	mm		
	Min	Nom	Max
A	2.20	2.30	2.40
A2	0.97	1.07	1.17
b	0.683 Tm0		

## Package Information

Symbol	mm		
	Min	Nom	Max
A	2.20	2.30	2.35
A1	0.90	1.01	



**OSG65R2KAF**  
Enhancement Mode N-Channel Power MOSFET 