

120V N-Ch Power MOSFET

Feature

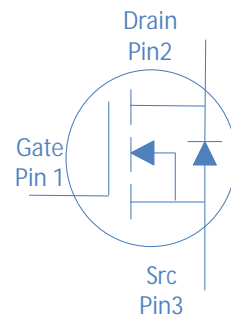
- High Speed Power Switching
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead Free

Application

- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit
- Power Tools
- UPS
- Motor Control

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|-------------------------|---------|-----|------------|
| V_{DS} | | 120 | V |
| $R_{DS(on),typ}$ | TO-220F | 8.3 | m Ω |
| I_D (Silicon Limited) | | 49 | A |

TO-220F



| Part Number | Package | Marking |
|-------------|---------|-----------|
| HGA100N12S | TO-220F | GA100N12S |

Absolute Maximum Ratings at $T_J=25$ (unless otherwise specified)

| Parameter | Symbol | Conditions | Value | Unit |
|--|----------------|-------------------|------------|------|
| Continuous Drain Current (Silicon Limited) | I_D | $T_C=25$ | 49 | A |
| | | $T_C=100$ | 35 | |
| Drain to Source Voltage | V_{DS} | - | 120 | V |
| Gate to Source Voltage | V_{GS} | - | ± 20 | V |
| Pulsed Drain Current | I_{DM} | - | 300 | A |
| Avalanche Energy, Single Pulse | E_{AS} | $L=0.4mH, T_C=25$ | 320 | mJ |
| Power Dissipation | P_D | $T_C=25$ | 43 | W |
| Operating and Storage Temperature | T_J, T_{stg} | - | -55 to 175 | |

Absolute Maximum Ratings

| Parameter | Symbol | Max | Unit |
|-------------------------------------|-----------------|-----|-------------|
| Thermal Resistance Junction-Case | $R_{\theta JC}$ | 3.5 | $^{\circ}W$ |
| Thermal Resistance Junction-Ambient | $R_{\theta JA}$ | 65 | $^{\circ}W$ |

Electrical Characteristics at $T_j=25$ (unless otherwise specified)

Static Characteristics

Parameter





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|---|---|
| Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage | Figure 8. Typical Capacitance vs. Drain-to-Source Voltage |
| Figure 9. Maximum Safe Operating Area | Figure 10. Maximun Drain Current vs. Case Temperature |
| Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case | |

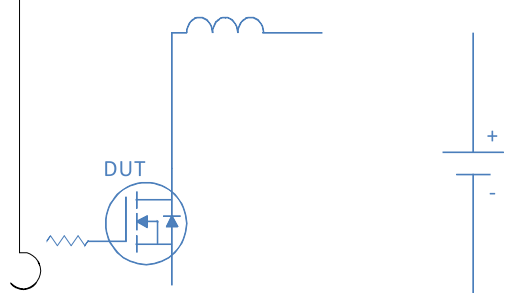
Inductive switching Test

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Gate Charge Test

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Uclamped Inductive Switching (UIS) Test

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|  <p>The diagram illustrates the UIS test circuit. It features a MOSFET labeled 'DUT' in a common-emitter configuration. The gate is driven by a pulse source. The drain is connected to a load inductor and a diode in parallel. The diode is connected to a DC source with its cathode to the drain and anode to ground. A resistor is connected between the gate and the drain.</p> | |
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Diode Recovery Test

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Package Outline

TO-220F, 3 leads

| DIM | MILLIMETERS |
|-----|-------------|
| A | 10.16 ± 0.3 |
| A1 | 7.00 ± 0.1 |
| A2 | 3.3 ± 0.2 |
| A3 | 9.5 ± 0.2 |
| B1 | 15.0 ± 0.3 |
| B2 | 4.0 ± 0.2 |
| B3 | 6.0 ± 0.4 |
| C | 3.0 ± 0.2 |
| C1 | 12.0 ± 0.3 |
| C2 | 10.0 ± 0.3 |
| D | 2.5 ± 0.05 |
| D1 | 1.0 ± 0.2 |
| D2 | 0.8 ± 0.1 |
| K | 3.0 ± 0.3 |
| E1 | 0.7 ± 0.2 |
| E2 | 0.3 ± 0.1 |

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 Unit:mm