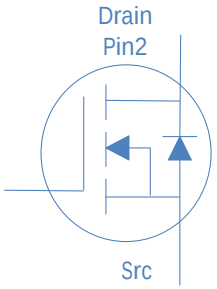
120V N-Ch Power MOSFET

V_{DS}		120	V
$R_{DS(on),typ}$	TO-252	8.6	mΩ
$I_{D\ (Sillicon\ Limited)}$		102	A
$I_{D\ (Package\ Limited)}$		70	A



Part Number	Package	Marking
HGD100N12S	TO-252	GD100N12S

Absolute Maximum Ratings at T_j=25 (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25	102	A
		T_C=100	72	
Continuous Drain Current (Package Limited)		T_C=25	70	
Drain to Source Voltage	V_{DS}	-	120	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	280	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.4mH, T_C=25	320	mJ
Power Dissipation	P_D	T_C=25	188	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to175	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Case	$R_{\theta JC}$	0.8	/W
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	/W

Electrical Characteristics at T_j=25 (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value min	Value typ	Value max	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	120	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	2	3	4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=120V, T_j=25	-	-	1	μA
		V_{GS}=0V, V_{DS}=120V, T_j=100	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	8.6	10	mΩ
Transconductance	g_{fs}	V_{DS}=5V, I_D=20A	-	65	-	S
		V_{GS}=0V, V_{DS} Open, f=1MHz	-	3.5	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}		-	4470	-	
Output Capacitance	C_{oss}	V_{GS}=0V, V_{DS}=60V, f=1MHz	-	235	-	pF
Reverse Transfer Capacitance	C_{rss}		-	9.5	-	
Total Gate Charge	Q_g		-	56	-	
Gate to Source Charge	Q_{gs}	V_{DD}=60V, I_D=20A, V_{GS}=10V	-	18	-	nC
Gate to Drain (Miller) Charge	Q_{gd}		-	6	-	
				16	-	
	t_r		-			
				38	-	

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=20A	-			

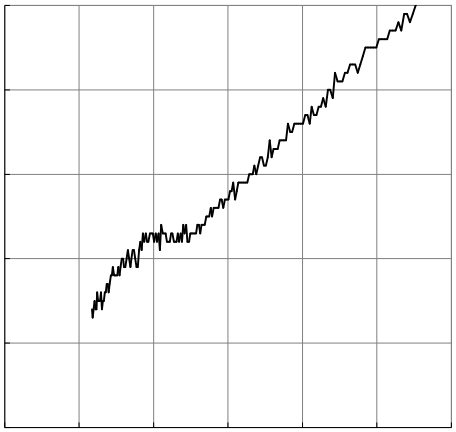
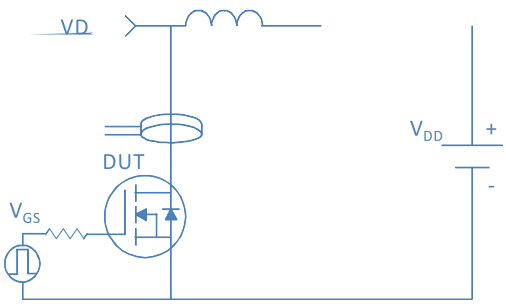
Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage	Figure 8. Typical Capacitance vs. Drain-to-Source Voltage
	

Figure 9. Maximum Safe Operating Area	Figure 10. Maximun Drain Current vs. Case Temperature

Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case

Inductive switching Test	

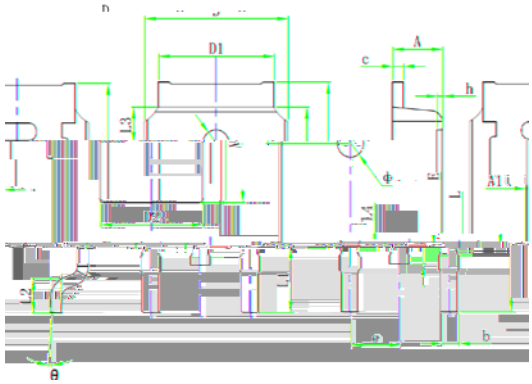
Gate Charge Test	

Uclamped Inductive Switching (UIS) Test	
	

Diode Recovery Test	

Package Outline

TO-252, 2 leads



Min.	Max.	Min.	Max.	Symbol	Min.	Max.
2.200	2.400	0.087	0.094	A		
0.000	0.127	0.000	0.005	A1		
0.660	0.860	0.026	0.034	b		
0.460	0.580	0.018	0.023	c		
6.500	6.700	0.256	0.264	D		
5.100	5.460	0.201	0.215	D1		
4.830 REF.		0.190 REF.		D2		
6.000	6.200	0.236	0.244	E		
2.186	2.386	0.086	0.094	e		
9.800	10.400	0.386	0.409	L		
2.900 REF.		0.114 REF.		L1		
1.400	1.700	0.055	0.067	L2		
1.600 REF.		0.063 REF.		L3		
0.600	1.000	0.024	0.039	L4		
1.100	1.300	0.043	0.051	Φ		
°	8°	0°	8°	θ	0	
00	0.300	0.000	0.012	h	0.0	
5.350 REF.		0.211 REF.		V		