100V N-Ch Power MOSFET

Feature

- High Speed Power Switching, Logic Level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested 100% Rg Tested
- Lead Free, Halogen Free

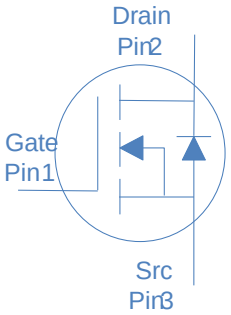
V_{DS}		100	V
$R_{DS(on),typ}$	V_{GS}=10V	9.0	mΩ
$R_{DS(on),typ}$	V_{GS}=4.5V	11	mΩ
$I_{D\ (Sillicon\ Limited)}$		73	A
$I_{D\ (Package\ Limited)}$		70	A

Application

- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit
- DC/DC in Telecoms and Industrial

TO-252

TO-251



Part Number	Package	Marking
HGD110N10SL	TO-252	GD110N10SL
HGI110N10SL	TO-251	GI110N10SL

Absolute Maximum Ratings at T_j=25 (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25	73	A
		T_C=100	52	
Continuous Drain Current (Package Limited)		T_C=25	70	
Drain to Source Voltage	V_{DS}	-	100	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	190	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.1mH, T_C=25	22	mJ
Power Dissipation	P_D	T_C=25	125	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to175	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	1.2	/W

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			-			S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	1.5	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}		-	2275	-	
Output Capacitance	C_{oss}	V_{GS}=0V, V_{DS}=50V, f=1MHz	-	162	-	pF
			-	7.9	-	
Total Gate Charge	Q_g(10V)		-	29	-	
Total Gate Charge	Q_g(4.5V)	V_{DD}=50V, I_D=14A, V_{GS}=10V	-	14	-	nC
Gate to Source Charge	Q_{gs}		-	5	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	5	-	
Turn on Delay Time	$t_{d(on)}$		-	8	-	
Rise time	t_r	V_{DD}=50V, I_D=14A, V_{GS}=10V,	-	3	-	ns
Turn off Delay Time	$t_{d(off)}$	R_G=10Ω,	-	26	-	
Fall Time	t_f		-	4	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=20A	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=50V, I_F=12A, dI_F/dt=500A/μs	-	33	-	ns
Reverse Recovery Charge	Q_{rr}		-	157	-	nC

Fig 1. Typical Output Characteristics

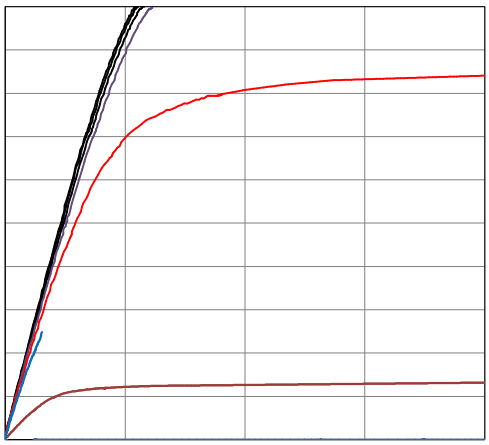


Figure 2. On-Resistance vs. Gate-Source Voltage

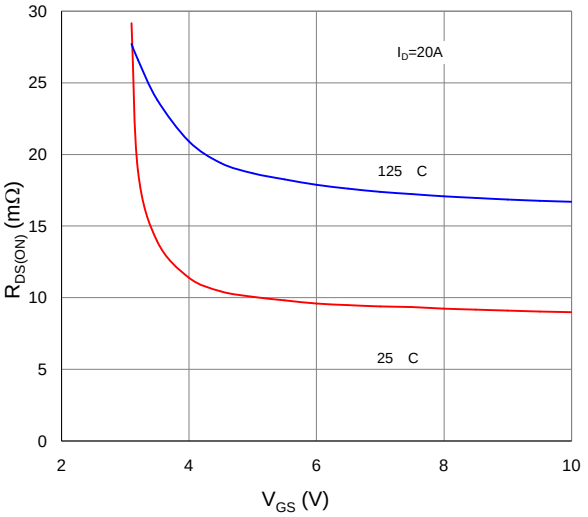


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

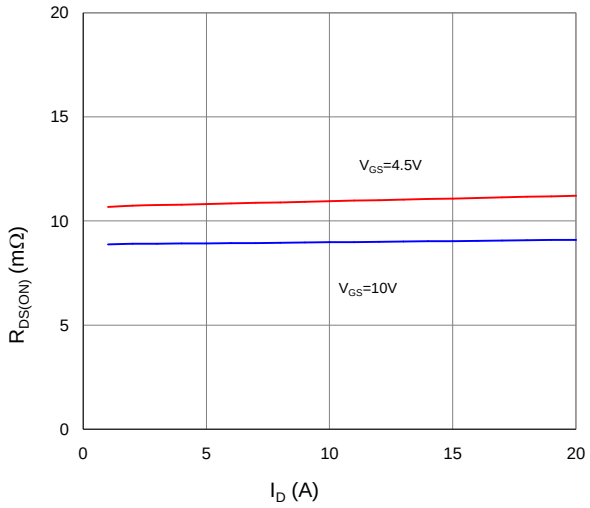


Figure 4. Normalized On-Resistance vs. Junction Temperature

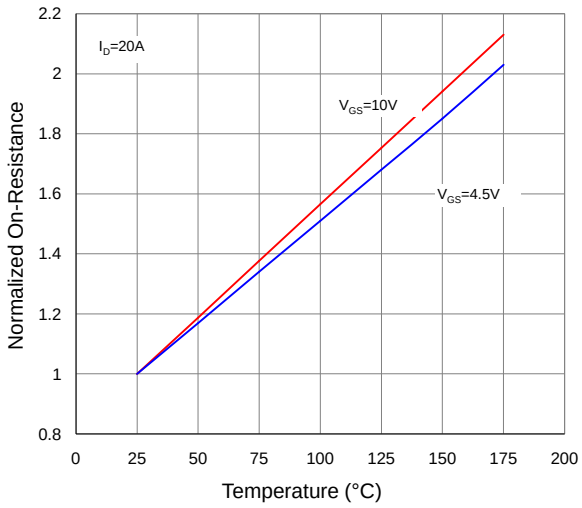


Figure 5. Typical Transfer Characteristics

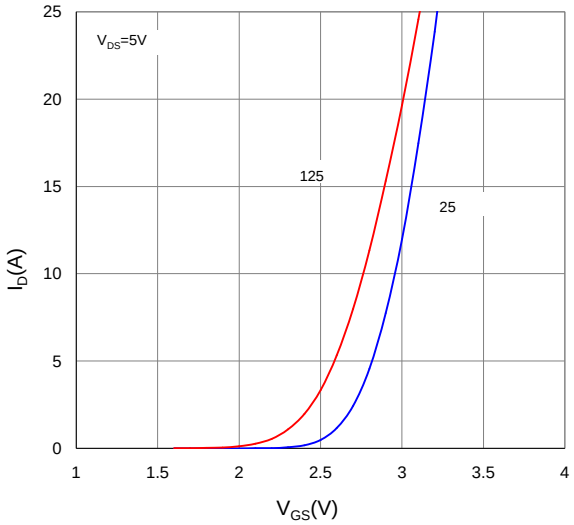


Figure 6. Typical Source-Drain Diode Forward Voltage

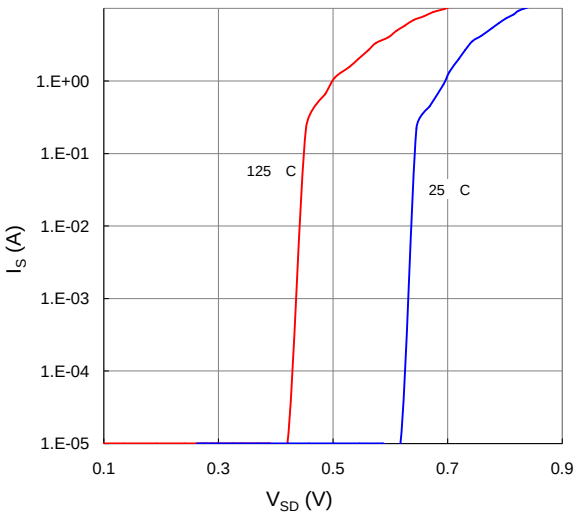


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

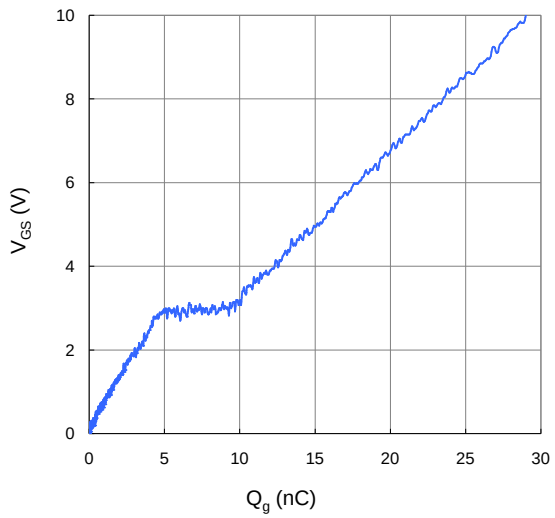


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

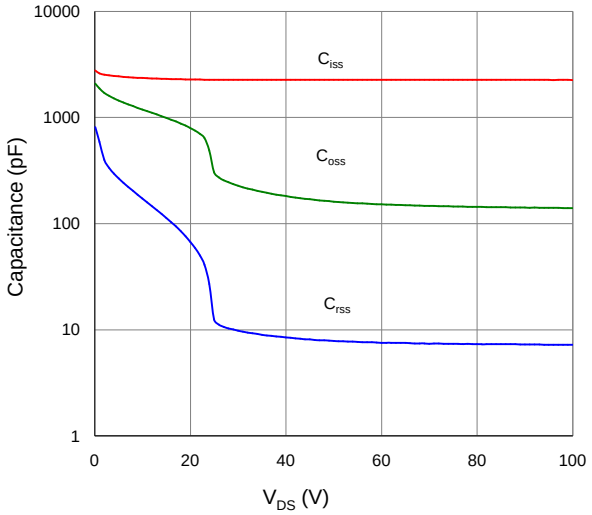


Figure 9. Maximum Safe Operating Area

Figure 10. Maximun Drain Current vs. Case Temperature

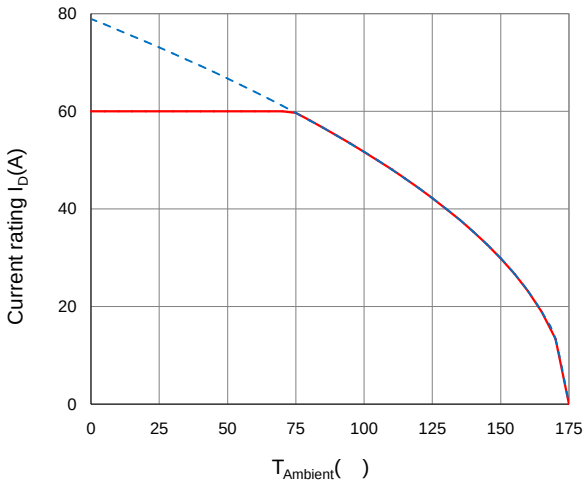
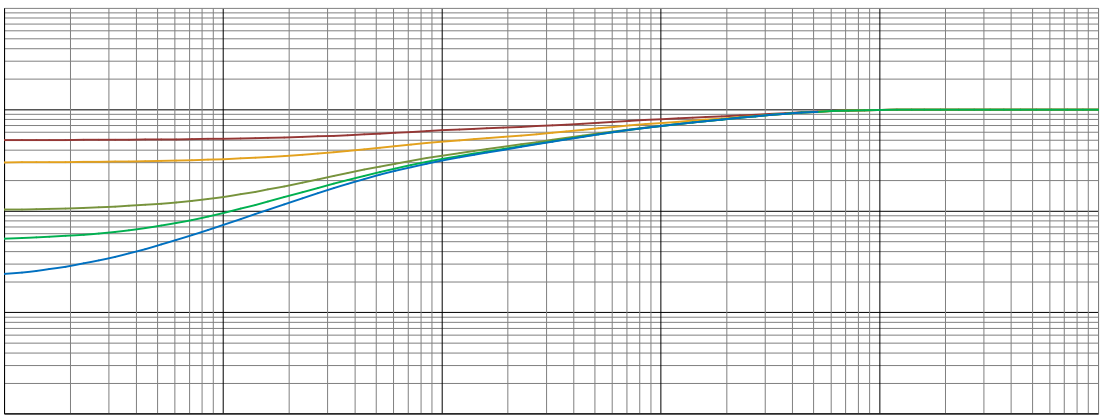


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



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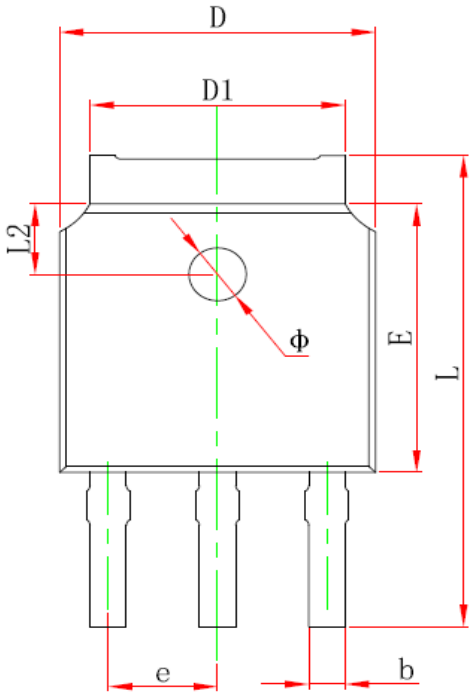
Charge Test

Inductive Switching (UIS) Test

Package Outline

TO-251, 3leads



Package Outline

TO-252, 2 leads