HGN080N08SL P-1

80V N-Ch Power MOSFET

Feature

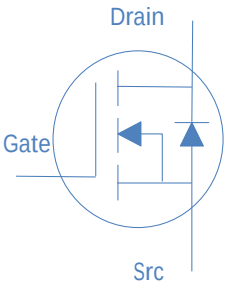
- High Speed Power Switching, Logic Level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead Free, Halogen Free

V_{DS}		80	V
$R_{DS(on),typ}$	V_{GS}=10V	6.3	mΩ
$R_{DS(on),typ}$	V_{GS}=4.5V	8.7	mΩ
$I_{D\ (Sillicon\ Limited)}$		85	A
$I_{D\ (Package\ Limited)}$		70	A

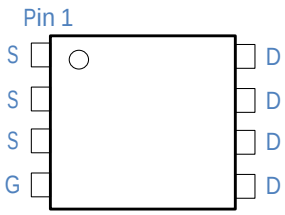
Application

- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit
- DC/DC in Telecoms and Inductrial

DFN5x6



Part Number	Package	Marking
HGN080N08SL	DFN5*6	GN080N08SL



Absolute Maximum Ratings at T_j=25 (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25	85	A
		T_C=100	60	
Continuous Drain Current (Package Limited)		T_C=25	70	
Drain to Source Voltage	V_{DS}	-	80	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	200	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.1mH, T_C=25	20	mJ
Power Dissipation	P_D	T_C=25	83	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 150	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	55	/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	1.5	/W

Electrical Characteristics at T_j=25 (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	80	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	1.0	1.6	2.4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=80V, T_j=25	-	-	1	μA
		V_{GS}=0V, V_{DS}=80V, T_j=100	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	6.3	8	mΩ
		V_{GS}=4.5V, I_D=20A	-	8.7	11.1	
Transconductance	g_{fs}	V_{DS}=5V, I_D=20A	-	65	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	1.5	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=40V, f=1MHz	-	2200	-	pF
Output Capacitance	C_{oss}		-	247	-	
Reverse Transfer Capacitance	C_{rss}		-	12.5	-	
Total Gate Charge	Q_g(10V)	V_{DD}=40V, I_D=20A, V_{GS}=10V	-	40	-	nC
Total Gate Charge	Q_g(4.5V)		-	19	-	
Gate to Source Charge	Q_{gs}		-	4.5	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	7.5	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=40V, I_D=20A, V_{GS}=10V, R_G=10Ω,	-	10	-	ns
Rise time	t_r		-	6	-	
Turn off Delay Time	$t_{d(off)}$		-	32	-	
Fall Time	t_f		-	8	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=20A	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=40V, I_F=20A, dI_F/dt=400A/μs	-	30	-	ns
Reverse Recovery Charge	Q_{rr}		-	90	-	nC

Fig 1. Typical Output Characteristics	Figure 2. On-Resistance vs. Gate-Source Voltage

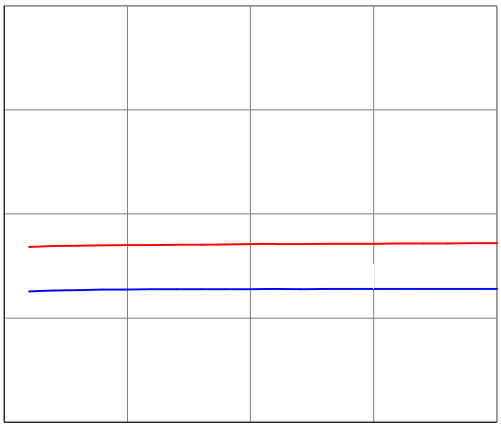
Figure 3. On-Resistance vs. Drain Current and Gate Voltage	Figure 4. Normalized On-Resistance vs. Junction Temperature
	

Figure 5. Typical Transfer Characteristics	Figure 6. Typical Source-Drain Diode Forward Voltage

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

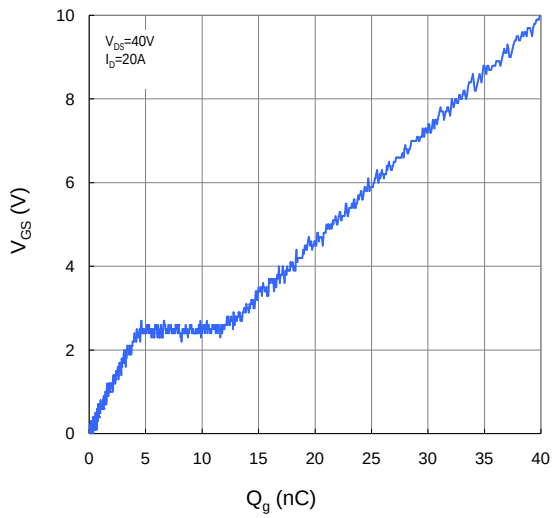


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

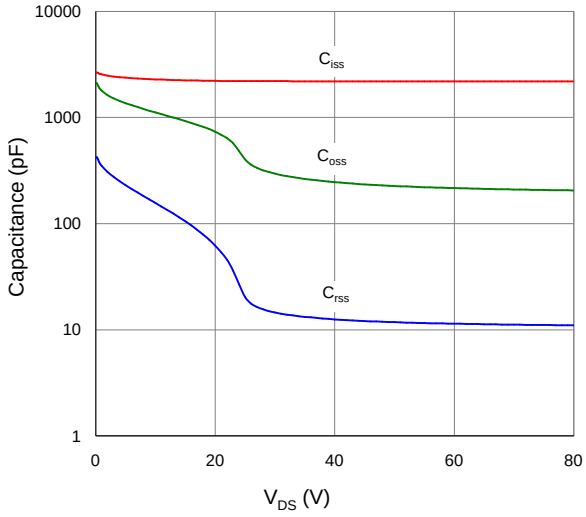


Figure 9. Maximum Safe Operating Area

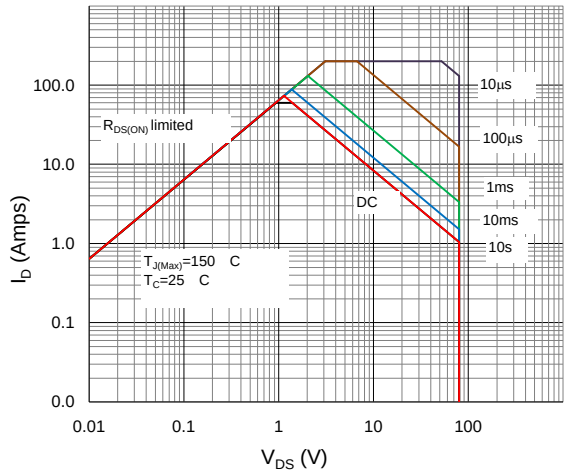


Figure 10. Maximun Drain Current vs. Case Temperature

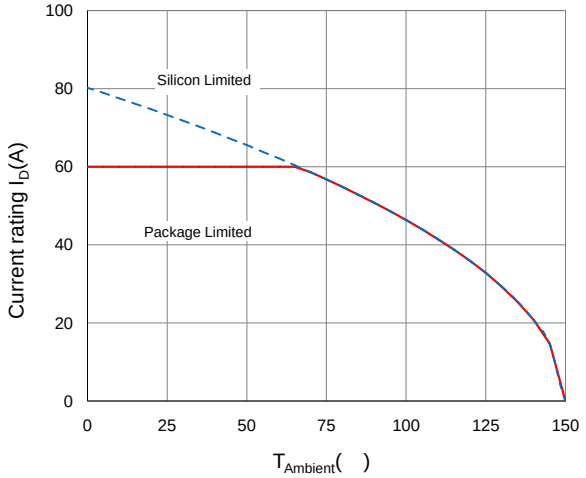
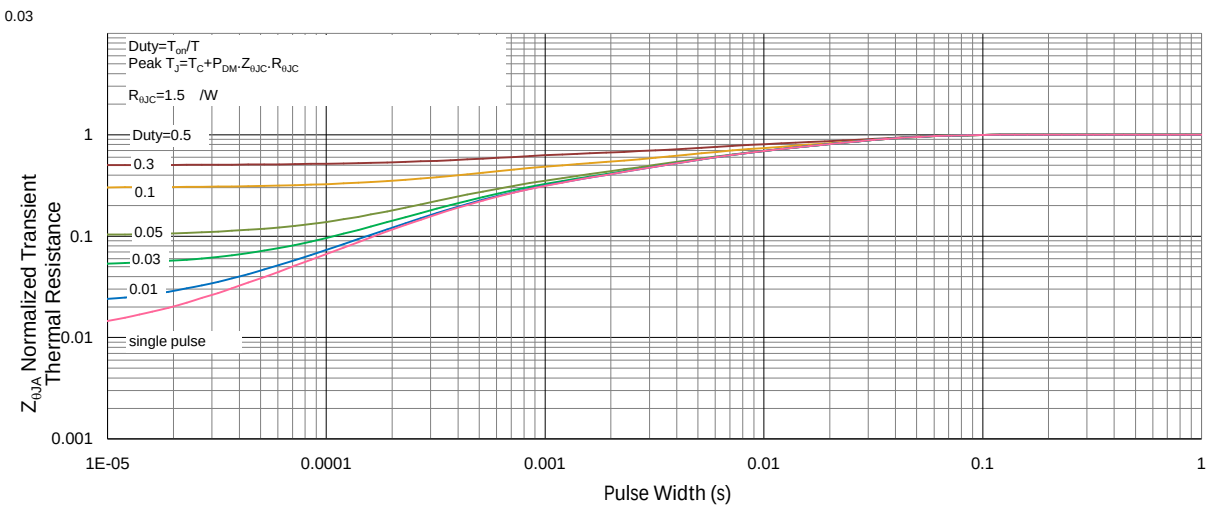


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



Inductive switching Test	

Gate Charge Test	

Uclamped Inductive Switching (UIS) Test	

Diode Recovery Test	