	V_{GS}=4.5V	12	mΩ
		47	A
$I_{D\ (Package\ Limited)}$		30	A

Part Number	Package
	DFN5*6

Parameter	Symbol		Value	
Continuous Drain Current (Silicon Limited)	I_D	T_C=100	30	
Continuous Drain Current (Package Limited)		T_C=25	30	
		-		V
		-		
		L=0.4mH, T_C=25	20	mJ

		Unit
$R_{\theta JA}$		/W
$R_{\theta JC}$		

Electrical Characteristics at T_j=25 (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	1.0	1.9	2.4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=60V, T_j=25	-	-	1	μA
		V_{GS}=0V, V_{DS}=60V, T_j=100	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=10A	-	8.5	11.5	mΩ
		V_{GS}=4.5V, I_D=8A	-	12	16	
Transconductance	g_{fs}	V_{DS}=5V, I_D=10A	-	25	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	1.5	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=30V, f=1MHz	-	1040	-	pF
Output Capacitance	C_{oss}		-	318	-	
Reverse Transfer Capacitance	C_{rss}		-	15	-	
Total Gate Charge	Q_g(10V)	V_{DD}=30V, I_D=10A, V_{GS}=10V	-	18.5	-	nC
Total Gate Charge	Q_g(4.5V)		-	9	-	
Gate to Source Charge	Q_{gs}		-	4.5	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	3.5	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=30V, I_D=10A, V_{GS}=10V, R_G=10Ω,	-	6	-	ns
Rise time	t_r		-	3	-	
Turn off Delay Time	$t_{d(off)}$		-	25	-	
Fall Time	t_f		-	3	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=20A	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=30V, I_F=10A, dI_F/dt=300A/μs	-	25	-	ns
Reverse Recovery Charge	Q_{rr}		-	33	-	nC

Fig 1. Typical Output Characteristics	Figure 2. On-Resistance vs. Gate-Source Voltage

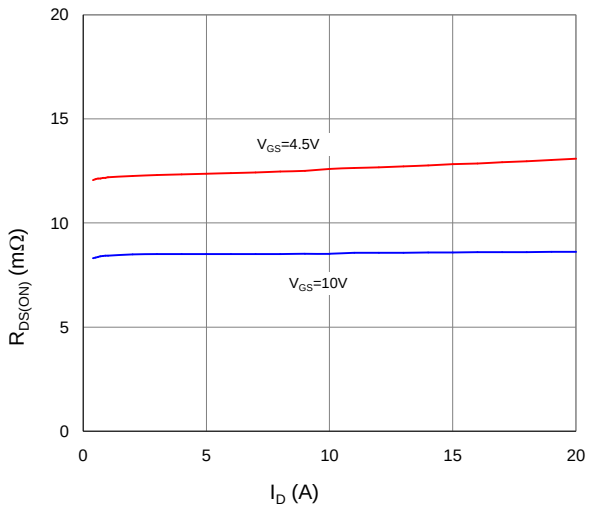
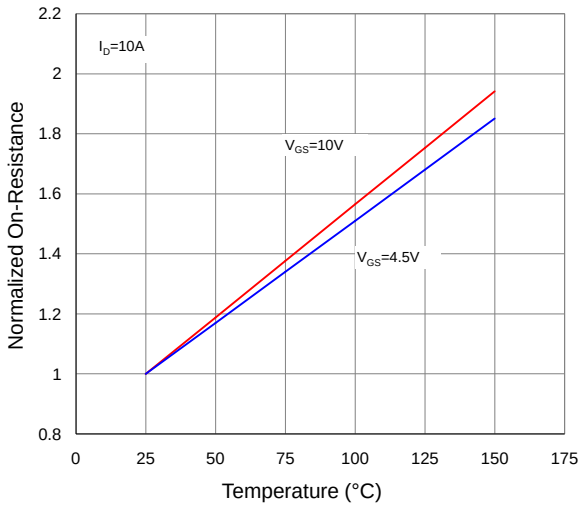
Figure 3. On-Resistance vs. Drain Current and Gate Voltage	Figure 4. Normalized On-Resistance vs. Junction Temperature
	

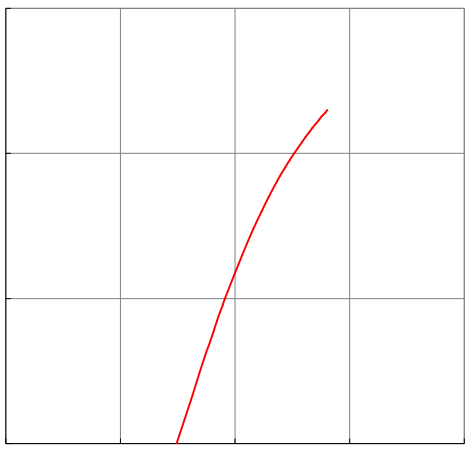
Figure 5. Typical Transfer Characteristics	Figure 6. Typical Source-Drain Diode Forward Voltage
	

Figure 7. Typ ate-Charge vs. Gate-to-Source Voltage	Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

Figure 9. Ma Safe Operating Area	Figure 10. Maximun Drain Current vs. Case Temperature

Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

Inductive switching Test	

rge Test

Package Outline

DFN5x6_P, 8 Leads